Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE431: Digital Integrated Circuits
Lab 2: CMOS Inverter Characteristics

Objectives:

Upon the completion of this Lab, you should be able to:
1. Run LVS on the inverter designed in the previous lab.
2. Test inverter voltage transfer characteristics of a CMOS inverter.
3. Design CMOS inverter for optimum transfer characteristics.
4. Evaluate the gate propagation delays then maximum input frequency.

Requirements:

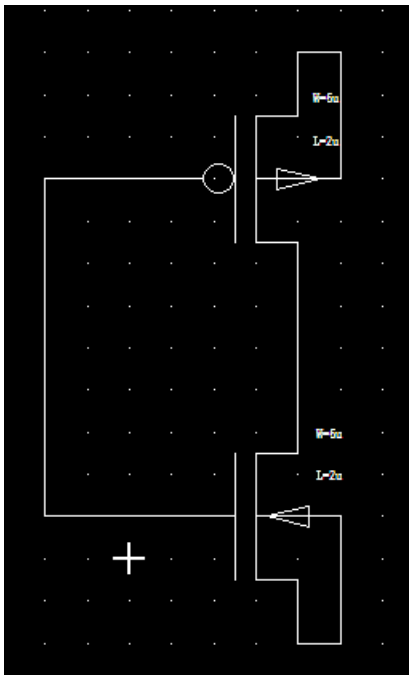
Lab 2 will expose students to procedure of LVS verification of layout. It will also expose students to the design CMOS inverter, draw VTC and change transistor sizing to see how it affects the VTC parameters. Then set the transistor sizing for optimum V_{th} such that $V_{th} = V_{DD}/2$ and optimize sizing again for having matched delays.

Change input frequency and observe the maximum input frequency.

Procedure:

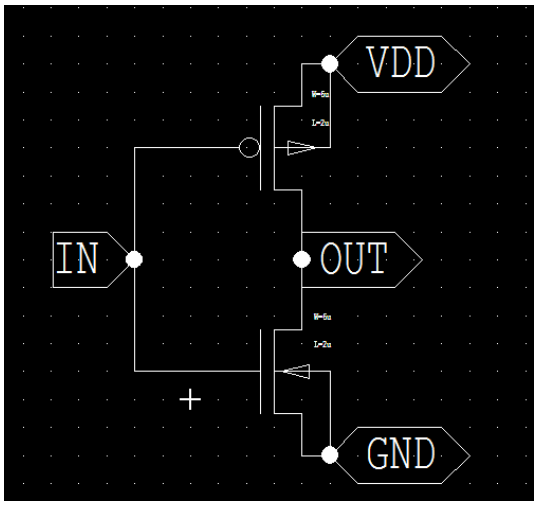
Part I: Layout Versus Schematic:

1. Open S-edit, and start drawing the inverter that was designed in Lab1.
2. The inverter schematic should be like this



(Note that the components can be added from symbol browser and wires can be added from the panel on the left)

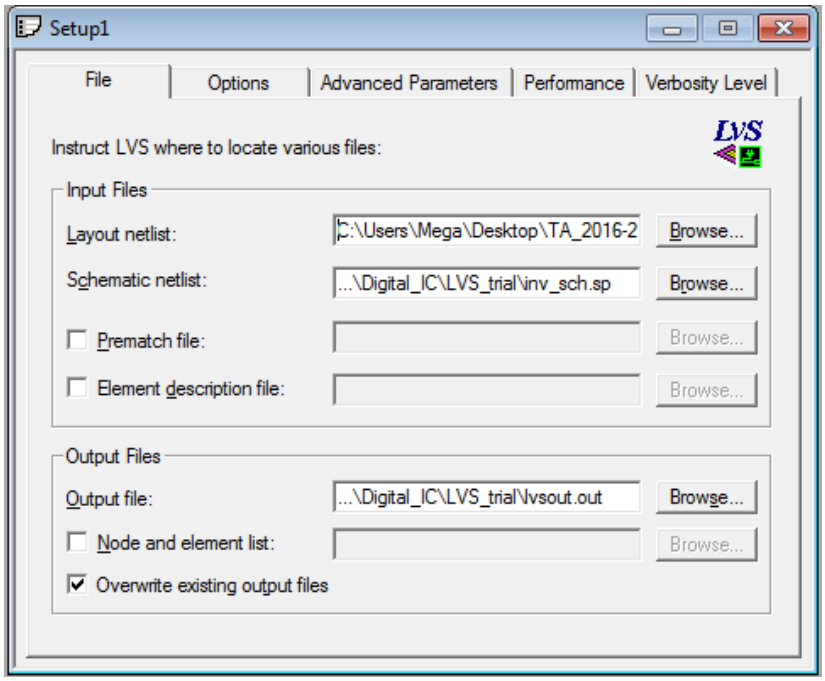
3. Add ports that are identical to the ones created in the layout.



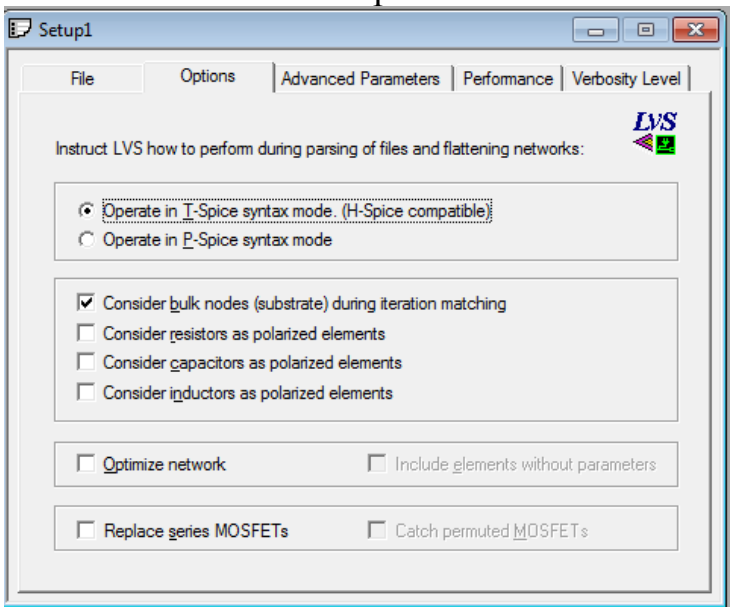
4. Click on the Tspice icon on the top panel.
5. A netlist has been created, save the netlist in a new folder where the technology file ml5_20 has been previously added.
6. Include the ml5_20 in the netlist.
7. Open the layout of the inverter and extract the netlist to the same folder.
8. Include ml5_20 in the layout netlist.

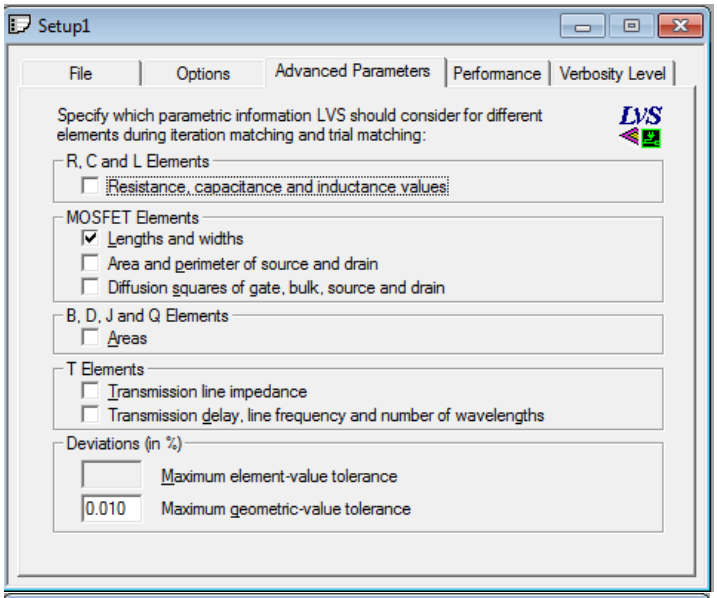
9. Open LVS, start new setup.

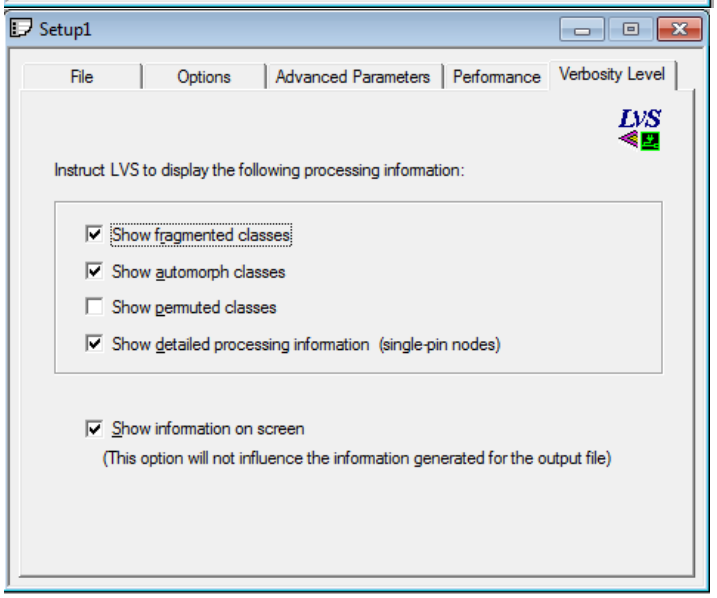
10. Add the layout and schematic netlists in their specified fields.



11. Make sure that the setup of the LVS is as follows.







12. Run LVS, if everything is correct, the LVS output log will write "*Circuits are equal*".

Part II Inverter Characteristics:

13. Use the created netlist from the schematic on T-spice,
14. Include ml2_20.md model instead of ml5_20, this model is level 2 so it will make calculations easier.
15. Place DC source (VDC) for V_{DD} and VPULSE for input.
16. Insert instructions for transient analysis. Print out the output and input voltages to see input and output waveforms. Figure 2.
17. Then choose the simulation type to be DC sweep. Sweep the input

voltage from 0 to V_{DD} to see VTC. Figure 3.

18. Change the sizing of transistors to get $V_{th} = V_{DD}/2$. You can refer to the model ml2_20.md for model parameters and the equations in the appendix for proper design.

19. Finally increase the input frequency until you get output waveform like the output waveform shown in figure 4.

20. Add a load capacitance of 1pF.

21. Measure τ_{PHL} and τ_{PLH}.

22. Resize the transistor so that τ_{PHL} and τ_{PLH} are equal.

Figure 1 CMOS inverter schematic

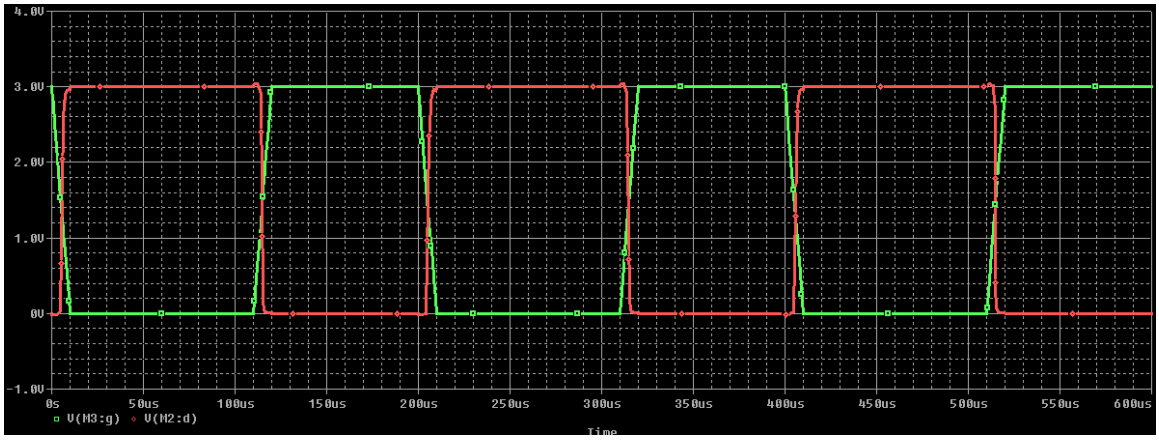


Figure 2CMOS inverter input and output waveforms

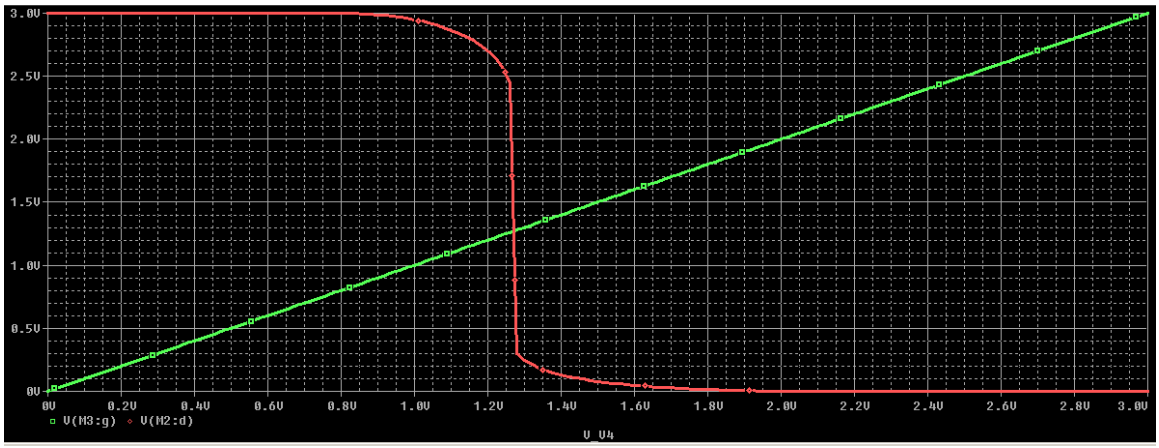


Figure 3 CMOS inverter VTC

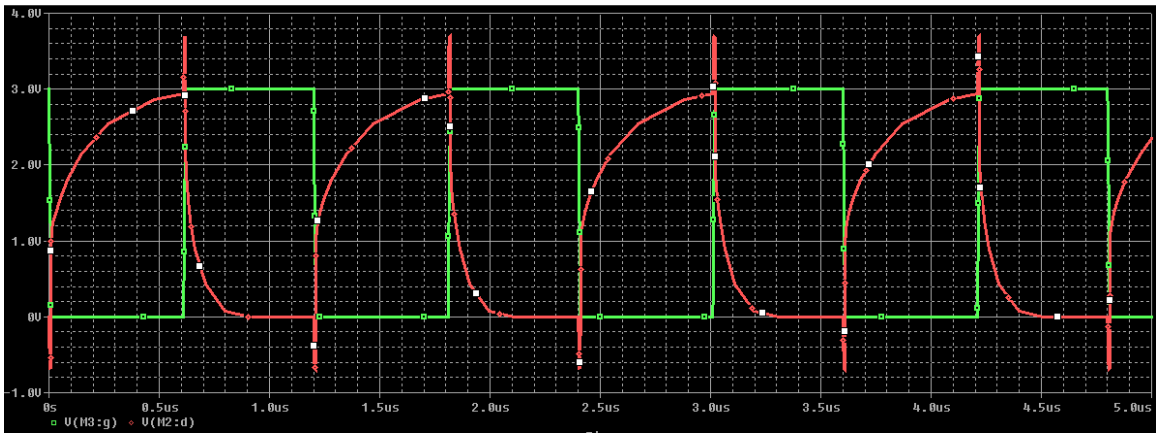


Figure 4 max input frequency and corresponding output waveform

Appendix:

Equations needed:

$$V_{th} = \frac{V_{T0,n} + \sqrt{\frac{1}{k_R}} \cdot \left(V_{DD} + V_{T0,p}\right)}{\left(1 + \sqrt{\frac{1}{k_R}}\right)}$$

$$\tau_{PHL} = \frac{C_{load}}{k_n \left(V_{DD} - V_{T,n}\right)} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1 \right) \right]$$

$$\tau_{PLH} = \frac{C_{load}}{k_p \left(V_{DD} - \left|V_{T,p}\right|\right)} \left[\frac{2\left|V_{T,p}\right|}{V_{DD} - \left|V_{T,p}\right|} + \ln\left(\frac{4\left(V_{DD} - \left|V_{T,p}\right|\right)}{V_{DD}} - 1 \right) \right]$$