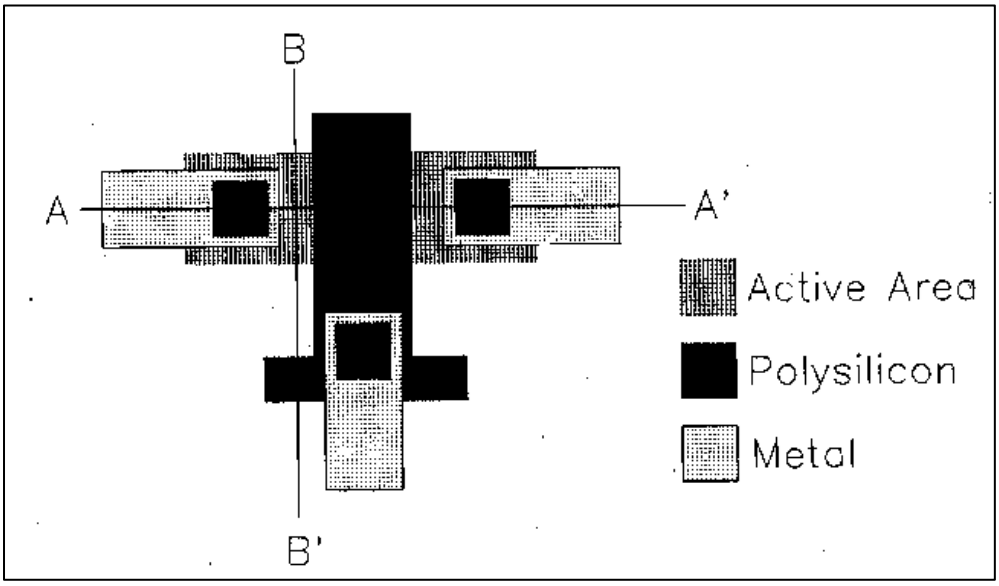
Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE431: Digital Integrated Circuits
Sheet 1: MOS Inverter Static Characteristics

1) Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The enhancement-type nMOS driver transistor has the following parameters:
   V_{DD}=5V, V_{T0} = 1V, $\gamma = 0.2V^{1/2}$, $\lambda = 0$, $\mu_n C_{ox} = 22\mu A/V^2$
   a. Determine the required aspect ratio
   b. Determine V_{IL} and V_{IH}
   c. Determine noise margins NM_L and NM_H.

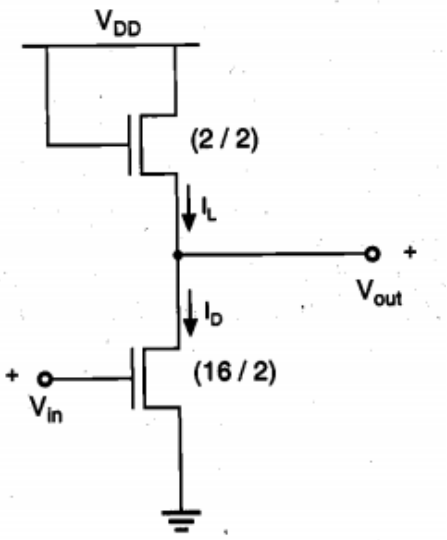
2) Draw the layout of the resistive-load inverter designed in Problem 1 using a polysilicon resistor with sheet resistivity of 25 Ω/square and the minimum feature size of 2 μm. It should be noted that L stands for the effective channel length which is related to the mask channel length as L = L_M + δ- 2 L_D. where we assume 8 (process error) = 0 and L_D = 0.25 μm. To save chip area, use minimum sizes for Wand L. Also, the circuit area can be reduced by using the folded layout (snake pattern) of the resistor.

3) Draw cross-sections of the following device along the lines A-A` and B-B`.



4) Consider the following nMOS inverter circuit which consists of two enhancement-type nMOS transistors, with the parameters:

$V_{T0} = 0.8$ V
$\mu_n C_{ox} = 45.0\ \mu A/V^2$
$\gamma = 0.38\ V^{1/2}$
$|2\ \phi_F| = 0.6$ V
$\lambda = 0$
$V_{DD} = 5.0$ V



5)
   a. Calculate V_{OH} and V_{OL} values. Note that the substrate-bias effect of the load device must be taken into consideration.
   b. Interpret the results in terms of noise margins and static (DC) power dissipation.
   c. Calculate the steady-state current which is drawn from the DC power supply when the input is a logic "1", i.e., when $V_{in} = V_{OH}$

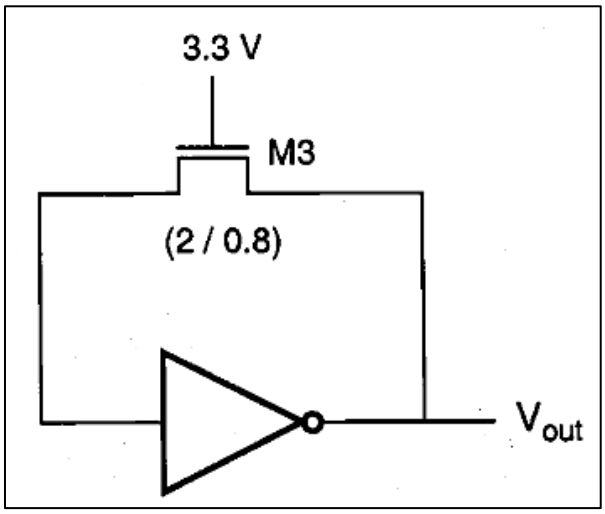
6) Design of a depletion-load nMOS inverter:
   V_{DD}=5V, V_{T0} = 0.8V (E-type), V_{T0} = -2.8V (D-type)
   $\gamma = 0.38V^{1/2}$, $\mu_n C_{ox} = 30\mu A/V^2$, $|2\Phi_F| = 0.6V$
   a. Determine the (WIL) ratios of both transistors such that:
      i. the static (DC) power dissipation for $V_{in} = V_{OH}$ is 250 µW, and
      ii. $V_{OL} = 0.3V$
   b. Calculate V_{IL} and V_{IH} values, and determine the noise margins.
   c. Plot the VTC of the inverter circuit.

7) Consider CMOS inverter with the following parameters:
   NMOS: $V_{T0,n} = 0.6$ V $\mu_n C_{ox} = 60\ \mu A/V^2$ $(W/L)_n = 8$
   PMOS: $V_{T0,p} = 0.7$ V $\mu_p C_{ox} = 25\ \mu A/V^2$ $(W/L)_p = 12$
   Calculate the noise margins and the switching threshold (V_{th}) of this circuit. The power supply is $V_{DD} = 3.3$ V.

8) Design of a CMOS inverter circuit:
   Use the same device parameters as in problem 6.
   The power supply $V_{DD} = 3.3$ V. The channel length of both transistors is $L_n = L_p = 0.8$ µm.

a) Determine the (W_n /W_p) ratio so that the switching (inversion) threshold voltage of the circuit is V_{th} = 1.4 V.
b) The CMOS fabrication process used to manufacture this inverter allows a variation of the $V_{T0,n}$ value by ±15% around its normal value, and a variation of the $V_{T0,p}$ value by ±20% around its normal value. Assuming that all other parameters (such as μ_n, μ_p, C_{ox}, W_n ,W_p) always retain their nominal values, find the upper and lower limits of the switching threshold voltage (V_{th}) of this circuit.

9) Consider the CMOS inverter designed in problem 7, with the following circuit configuration



a) Calculate the output voltage level V_{out}.
b) Determine if the process-related variation of $V_{T0,n}$ of M3 has any influence upon the voltage V_{out}.
c) Calculate the total current being drawn from the power supply source, and determine its variation due to process-related threshold voltage variations.

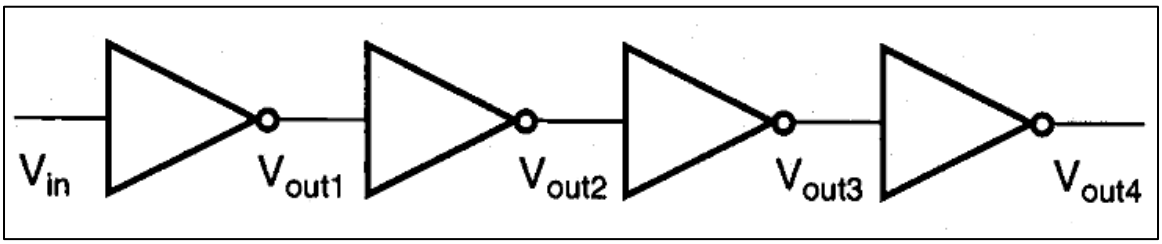
10) Consider a CMOS inverter, with the following device parameters:

NMOS: $V_{T0,n}$ = 0.6 V $\mu_n C_{ox}$ = 60 μA/V^2
PMOS: $V_{T0,p}$ = - 0.8 V $\mu_p C_{ox}$ = 20 μA/V^2
Also consider: V_{DD} = 3 λ = 0

a) Determine the (W/L) ratios of the NMOS and the PMOS transistor such that the switching threshold is V_{th} = 1.5 V.
b) Plot the VTC of the CMOS inverter using SPICE.
c) Determine the VTC of the inverter for λ = 0.05 and λ = 0.1 V^{-1}.
d) Discuss how the noise margins are influenced by non-zero λ value. Note that transistors with very short channel lengths tend to have

larger λ values than long-channel transistors.

11) Consider the CMOS inverter designed in problem 9 above, with $\lambda = 0.1\ V^{-1}$. Now consider a cascade connection of four identical inverters, as shown.



a) If the input voltage is $V_{in} = 1.55$ V, find V_{out1}, V_{out2}, V_{out3} and V_{out4}. (note that this requires solving KCL equations for each subsequent stage, using the non-zero λ value).
b) How many stages are necessary to restore a true logic output level?
c) Verify your result with SPICE simulation.