Alexandria University
Faculty of Engineering
Electrical Engineering Department

EE 431: Digital Integrated Circuits
Sheet 4 Combinational Logic Circuits

1) Calculate the equivalent $\frac{W}{L}$ of the two NMOS with $\frac{W_1}{L}$ and $\frac{W_2}{L}$ connected in series. For simplicity, neglect the body effect, i.e., the threshold voltages of individual transistors are constant and do not depend on the source voltages. Although this is not true in reality, such an assumption is necessary for simple analysis with a reasonably good approximation.

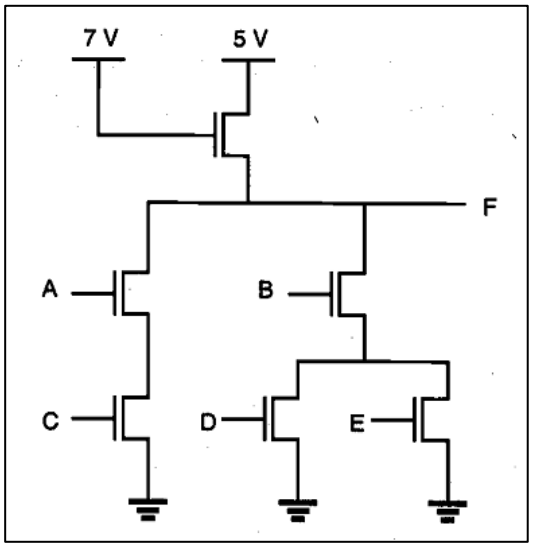
2) Analytical expressions for V_{th} (logic) have been derived in Chapter 7 for the CMOS NOR2 gate. Now consider the CMOS NAND2 gate for the following cases and use $k_p = k_n = 100\ \mu A/V^2$
   - two inputs switching simultaneously
   - top NMOS switching while the bottom NMOS's gate is tied to VDD
   - top NMOS gate is tied to VDD and the gate input of the bottom NMOS is changing.

   a) Derive an analytical expression for V_{th} corresponding to the first case. Also find the V_{th} value for the first case for VDD= V when the magnitudes of the threshold voltages are 1 V with y = 0.
   b) Determine Vth for all three cases by using SPICE.
   c) For C_{load} = 0.2 pF, calculate 50% delays (low-to-high and high-to-low propagation delays) for an ideal pulse input signal for each of the three cases by assuming that C_{load} includes all of the internal parasitic capacitances. Verify the results using SPICE.

3) For the gate shown in Figure,

   - Pull-up transistor ratio is 5/5
   - Pull-down transistor ratios are 100/5
   - V_{T0} = 1.0 V
   - $\gamma = 0.4\ V^{\frac{1}{2}}$
   - $|2\ \emptyset_F|$ = 0.6 V

   a) Identify the worst-case input combination(s) for V_{OL}.
   b) Calculate the worst-case value of V_{OL}. (Assume that all pull-down transistors have the same body bias and initially, that V_{OL} 5% VDD.)

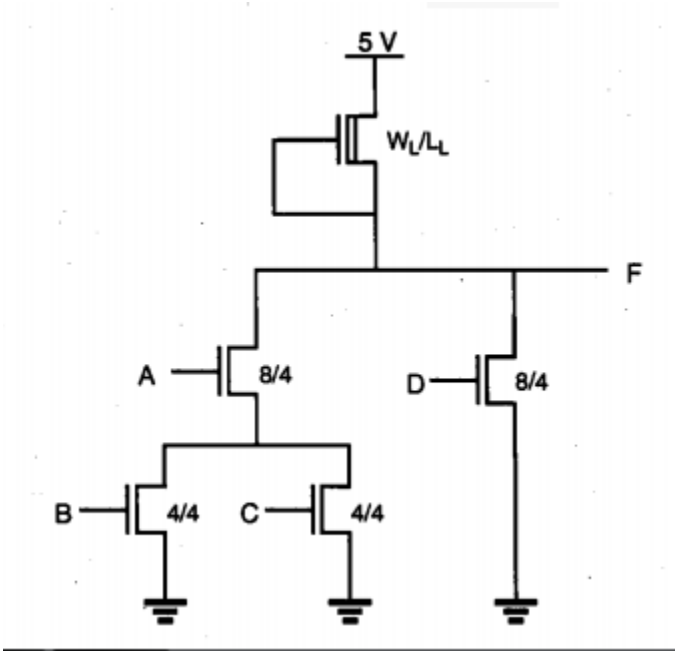


4) Calculate V_{OL}, V_{OH}, V_{IL}, V_{IH}, NM_L, and NM_H for a two-input NOR gate fabricated with CMOS technology.

$(W/L)_p = 4$, $(W/L)_n = 1$, $V_{Tn} = 0.7$ V, $V_{TP} = -0.7$ V,
$\mu_n C_{ox} = 40\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $V_{DD} = 5$ V

Compare your answers with SPICE simulation results.

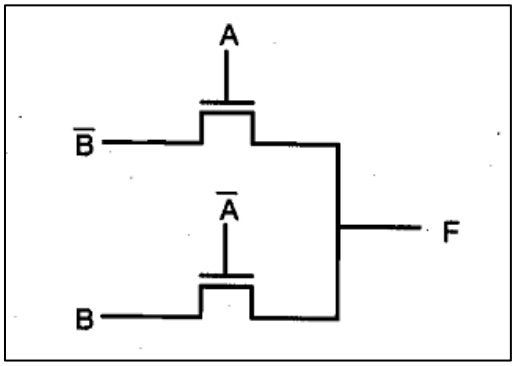
5) Consider the logic circuit shown in the following figure, with V_{TO}(enhancement) = 1 V, V_{TO}(depletion) = - 3 V, and $\lambda = 0$
   a. Determine the logic function.
   b. Calculate the size W_L/L_L such that V_{OL} does not exceed 0.4 V.
   c. Qualitatively, would W_L/L_L increase or decrease if the same conditions in (b) are to be achieved but $\lambda = 0.4\ V^{1/2}$?



6) The enhancement-type MOS transistors have the following parameters:
VDD = 5 V
$|V_{T0}| = 1.0$ V for both nMOS and pMOS transistor
$\lambda = 0.0\ V^{-1}$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $\mu_n C_{ox} = 50\ \mu A/V^2$
For a CMOS complex gate OAI432 with $(W/L)_p = 30$ and $(W/L)_n = 40$:
   a. Calculate the W/L sizes of an equivalent inverter with the weakest pull-down and pull-up. Such an inverter can be used to calculate worst-case pull-up and pull-down delays, with proper incorporation of parasitic capacitances at internal nodes into the total load capacitance. In this problem, you are asked to calculate only $(W/L)_{worse\ case}$ for both p-channel and n-channel MOSFETs by neglecting the parasitic capacitances.

b. Do the layout of OAI432 with minimal diffusion breaks to reduce the number of polysilicon column pitches. With proper ordering of polysilicon gate col-umns, the number of diffusion breaks can be minimized. One way of achieving such a goal is to find a Euler path common to both p-channel and n-channel nets using graph models. Symbolic layout that shows source and drain connections is sufficient to answer this problem.

7) Consider the circuit shown in the following Figure

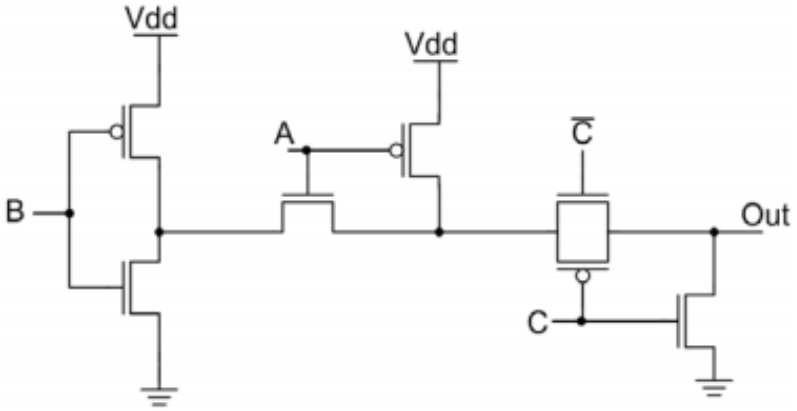


   a) Determine the logic function F.
   b) Design a circuit to implement the same logic function, but using NOR gates. Draw a transistor-level schematic and use NMOS E-D technology.
   c) Design a circuit to implement the same logic function, but use an
   d) AOI (AND-OR-INVERT) gate. Draw a transistor-level schematic and use, CMOS technology.

8) Consider a fully complementary CMOS transmission gate with its input terminal tied to ground (0 V) while the other non-gate terminal is tied to a 1 pF load capacitor initially charged to 5 V. At t = 0, both transistors are fully turned on by clock signals to start the discharge of the capacitor.
   - $|V_{T0}| = 1\,V$
   - $\mu_p C_{ox} = 20\ \mu A/V^2$
   - $\mu_n C_{ox} = 50\ \mu A/V^2$

   a) Plot the effective resistance of this transmission gate as a function of capacitor voltage when $(W/L)_p = 50$ and $(W/L)_n = 40$. From the plot find the average value of the resistance. Then calculate the RC delay for the capacitor voltage to change from 5 V to 2.5 V. This can be found by solving the RC-circuit differential equation.

9) Someone claims they have implemented a static CMOS gate with the circuit shown below. In order to find the problem with this gate, using the switch model, fill in a table showing the voltage (i.e., Vdd, Gnd, Vth, etc.) at Out for all possible combinations of the inputs A, B, and C. In other words, you should fill out the "truth table" for the gate, but with voltages instead of ones and zeros.



10) By adding just one more transistor to the circuit shown above, fix the circuit so that it will indeed implement a static gate. What is the logic function of this gate. Note that you are free to use both the true and complement versions of the input signals (A, B, and C) to achieve this.

11)

a. Implement the function $F = \overline{AD(C + B)}$. Assuming long-channel transistors, size the devices so that the worst-case drive resistance is the same as an inverter with $W_N/L = 2$ and $W_P/L = 4$.
b. Imagine that input "B" to the gate was always the last one to arrive, making the delay of the gate from B rising or falling to the output falling or rising critical. Please re-arrange the implementation of your gate so that the delay of the gate from B transitioning is minimized.
c. Draw a stick diagram of the gate you designed for part b) - you should minimize the diffusion breaks and use a single piece of poly for each input.
d. Now resize the gate to match the worst-case pull-up and pull-down resistances using the velocity saturated model. What is the LE from the B input?