Overloaded CDMA Interconnect for Network-on-Chip (OCNoC)

Khaled E. Ahmed, Mohamed R. Rizk, Mohammed M. Farag
Electrical Engineering Department, Faculty of Engineering, Alexandria University, Alexandria, Egypt
Email: k.e.elsayed@ieee.org, mrmrizk@ieee.org, mmorsy@alexu.edu.eg

***Abstract*—Networks on Chip (NoCs) have replaced on-chip buses as the paramount communication strategy in large scale Systems-on-Chips (SoCs). Code Division Multiple Access (CDMA) has been proposed as an interconnect fabric that can achieve high throughput and fixed transfer latency as the network nodes can transfer packets concurrently. Overloaded CDMA Interconnect (OCI) is an architectural evolution of the conventional CDMA interconnects that can double their bandwidth at marginal cost. Employing OCI in CDMA-based NoCs has the potential of providing higher bandwidth at low-power and -area overheads compared to other NoC architectures. Furthermore, fixed latency and predictable performance achieved by the inherent concurrency of CDMA can reduce the effort and overhead required to implement QoS.**

In this work, we advance the Overloaded CDMA interconnect for Network on Chip (OCNoC) dynamic central router. The OCNoC router leverages the overloaded CDMA concept to reduce the overall packet transfer latency and improve the network throughput at a negligible area overhead. Dynamic code assignment is adopted to reduce the decoding complexity and transfer latency. Two OCNoC solutions are advanced, serial and parallel CDMA encoding schemes. The OCNoC central routers are implemented and validated on a Virtex-7 VC709 FPGA kit. Evaluation results show a throughput enhancement up to 142% with a 1.7% variation in packet latencies. Synthesized using a 65 *nm* ASIC standard cell library, the presented OCNoC router requires 61% less area per processing element at 81.5% saving in energy dissipation.

***Keywords*—NoC, SoC, CDMA Interconnect, Central Router.**

I. Introduction

Buses and Networks-on-Chips (NoCs) are the most deployed topologies for interconnecting processing elements (PEs) in modern System-on-Chips (SoCs) [1]. In NoCs, data is bundled into packets, the PEs are interconnected via network nodes, routers, and crossbar switches. NoCs can provide a scalable on-chip communication solution for large SoCs but they exhibit increased power consumption and large resource overheads [2]. The crossbar switches in NoCs are the backbone of the network physical layer while routing algorithms and the network topologies constitute the higher network protocol layers that leverage the physical layer infrastructure to enable communications between on-chip PEs. The main switching techniques employed by NoC crossbars are Time Division Multiple Access (TDMA) and Space Division Multiple Access (SDMA). In TDMA, the interconnect media is time shared between router ports, while in SDMA, a dedicated link is established between interconnected ports.

Code Division Multiple Access (CDMA) is another switching technique that leverages orthogonal codes to enable simultaneous packet routing. CDMA has been proposed as an on-chip interconnect enabler for both bus and NoC architectures [3]. Many advantages of using CDMA for on-chip interconnects include reduced power consumption, fixed communication latency, and reduced system complexity [4]. The CDMA crossbars are characterized by lower wiring density and complexity than SDMA crossbars while incurring less packet transfer latency and higher throughput compared to TDMA crossbars. However, the use of CDMA interconnects in NoC routers has not been deeply explored in the SoC literature.

The capacity of CDMA crossbars is limited by the number of orthogonal spreading codes used to encode and decode NoC packets. Overloaded CDMA is a medium access scheme deployed in wireless communications where the number of nodes sharing the communication channel is increased by increasing the number of usable spreading codes at the expense of increasing Multiple Access Interference (MAI) [5]. In [6], overloaded CDMA is applied to classical SoC buses to improve the CDMA bus capacity. In this work, we apply the overloaded CDMA concept to NoC crossbars and advance the overloaded CDMA-based NoC (OCNoC) central router architecture. Two OCNoC solutions employing the Overloaded CDMA interconnect (OCI) are introduced with different area-latency profiles. To compare with existing CDMA-based NoCs, the OCNoC routers are synthesized using a 65 *nm* ASIC standard cell library. Moreover, the OCNoC routers are implemented and validated on a Virtex-7 VC709 FPGA kit.

Contemporary SoC designs heavily rely on reconfigurable hardware platforms due to their enhanced performance and flexibility features. Modern FPGAs can host a large number of heterogeneous coarse-grained IP cores such as soft processors, DSPs, memory controllers, and hardware accelerators which are interconnected in a hierarchical fashion to implement complex SoCs. The choice of the communication fabrics affects the overall area, performance, and energy efficiency of the SoC design. Compared to existing on-chip interconnects, the OCNoC router can meet the timing and performance requirements of modern SoC designs hosted on reconfigurable hardware while minimizing resource usage and power consumption.

The remaining of this paper is organized as follows: related work is presented in Section II. Preliminaries of the conventional, parallel, and overloaded CDMA crossbars are presented in Section III. The OCNoC router high-level architecture is advanced in Section IV. Performance evaluation of the OCNoC routers in terms of area, latency, throughput, and energy consumption is introduced in Section V. Conclusions and future work are portrayed in Section VI.

II. Related Work

The classical CDMA medium access scheme relies on the Walsh-Hadamard orthogonal code family to enable interconnect sharing. Using CDMA as a medium access scheme in NoCs provides several advantages like the fixed transaction latency and low arbitration overhead. A CDMA-based NoC has been compared to a PTP bidirectional ring-based NoC in [7], the comparison shows that the CDMA NoC's fixed data transfer latency is equal to the best case latency of the PTP NoC of the same channel width due to the concurrent sharing of the communication channel by network nodes. A hierarchical CDMA star NoC router has been compared to pure mesh and fat tree topologies in [8], [9]. The CDMA star NoC exhibits fewer resources and routing complexity than its rivals with less maximum hop count due to the concurrent transmission of packets through the CDMA router.

In [6], two OCI bus architectures have been presented, the OCI buses employ orthogonal Walsh codes and overloaded, non-orthogonal codes. The addition of the non-orthogonal codes to the code set improves the achievable throughput of the bus at a marginal overhead. The number of overloaded codes is equal to the number of orthogonal codes, thus, the achievable throughput of the OCI is double that of conventional CDMA-based buses. A 14-node CDMA-based network has been developed in [10]. The 14 nodes are connected by a central router employing fixed priority arbitration. The PEs transmit packets with sizes up to 256 bits divided into flits of 16 bits each. The assignment of codes to transmit-receive pairs is dynamic based on the node request. Two architectures have been introduced: a serial CDMA NoC where each chip in the spreading code is sent in one clock cycle on a single wire; and a parallel CDMA NoC where all spreading chips are sent in the same cycle using multiple wires. The serial and parallel CDMA NoCs have been compared with a conventional CDMA NoC, a mesh-based NoC, and a TDMA bus. For the same network area, the throughput of the parallel CDMA network is higher than that of the mesh-based NoC and TDMA bus due to the simultaneous medium access nature of CDMA. In this work, we propose to boost the throughput of the dynamic CDMA NoC of [10] by adopting the OCI concepts presented in [6].

III. CDMA Interconnect Preliminaries

A. Conventional CDMA Crossbar

This section presents preliminaries of CDMA for on-chip interconnects. The block diagram of the conventional CDMA crossbar is shown in Figure 1. The conventional CDMA crossbar interconnects M transmit-receive pairs, where M is equal to $N-1$. The CDMA crossbar is composed of CDMA encoders, decoders, and a binary adder. In the encoder, an N-chip length binary orthogonal code, generated from the Walsh code family, is XORed with the transmitted data bit and sent out serially. Therefore, the encoder spreads each data bit into N bits in a period of N clock cycles. Serial encoded streams from all transmitting cores sharing the channel are added together and the sum is sent to each decoder. In the conventional CDMA encoding-decoding scheme relying solely on orthogonal spreading codes, the adder has $M = N-1$ input bits and $m = \log_2 N$ output bits.

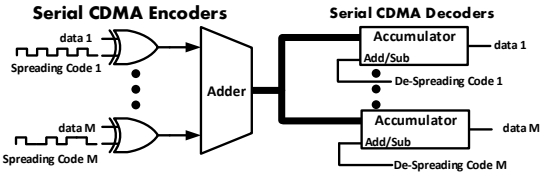

Fig. 1. Conventional CDMA crossbar architecture [6]

The decoder cross correlates the received CDMA sum with the signature code by which the data is encoded. In CDMA, due to the orthogonality property, code cross correlation yields zero while auto correlation yields N. Encoding and decoding a serial CDMA stream requires N clock cycles. Because the spreading codes are binary, the multiply-add operation of the cross-correlator can be realized by an up/down accumulator circuit. The accumulator adds the CDMA sum value to its accumulated value when the spreading code chip is equal to "0" but subtracts the two values when the spreading code chip is equal to "1". The accumulator is reset to zero at the beginning of each decoding cycle. At the end of the decoding cycle, the accumulator holds the sum of the spreading codes or their complements encoded according to the data sent by the transmit ports. The decoded data is the inverse of the sign bit of the accumulated value, a positive accumulated value indicates that the encoded data bit is "1", while a negative accumulated value represents a "0". Consequently, the accumulator decoder is a cost-efficient method to implement the cross-correlator decoder required by the CDMA technique [11].

As illustrated in Figure 1, the encoding and decoding of data in the CDMA interconnect is conducted in a serial fashion. In a serial transmission, the CDMA code is sent serially to an XOR gate to be XORed with the transmitted data bit, the encoded data is sent to the decoder and this process is repeated every N clock cycles. Another method to encode and decode data by CDMA codes is the parallel scheme in which all CDMA code chips are XORed with the data to be spread in parallel using multiple wires. Therefore, the XOR gate at each encoder is replicated N times, the CDMA adder is replicated N times as well to add the encoded CDMA bits in parallel. The decoder is modified, however, from being an accumulator decoder into a parallel adder decoder. The adder output from all parallel encoded bits are either added or subtracted based on the despreading code value.

B. Overloaded CDMA Interconnect

As this work employs the OCI scheme presented in [6], we dedicate this section to present the OCI preliminaries. In the conventional CDMA interconnect, the encoded stream of each data bit is the result of XORing the bit with an orthogonal CDMA code. The CDMA sum stream is the bit-by-bit summation of data spread by the orthogonal codes. Consequently, when a data bit is negated, its spread data is also negated. However, the difference between each consecutive CDMA sum values remains even, regardless of the value encoded by each transmit port. This is because the Walsh orthogonal codes are balanced (the number of "1" chips in each code is equal to the number of "0"chips), therefore, flipping a spreading code does not change the interrelation between the channel sum values. The even difference between consecutive CDMA sum values is a featured property of Walsh codes that enables augmenting an orthogonal spreading code set by a

significant number of identifiable non-orthogonal spreading codes. An overloading ratio of 100% can be achieved by encoding data in the $N-1$ consecutive sum values for an N-chip length Walsh code set.

To encode data in the difference between consecutive sums, non-orthogonal spreading codes can be used to alter the parity of that difference. The non-orthogonal code either keeps the difference even or makes it odd, according to the encoded data. To achieve this, the non-orthogonal code will comprise a single "1" chip and the remaining $N-1$ chips are set to zero. Non-orthogonal encoders encode transmit data using an AND gate instead of the XOR encoder. Therefore, for a non-orthogonal encoder, if the transmitted data bit is one, a single "1" chip is added to the CDMA sum at a specific time slot in the spreading cycle. This causes the difference between consecutive sums to deviate from its nominal even value. The non-orthogonal codes imitate the TDMA signaling scheme as each code includes a single chip of "1" which is sent in a specific time slot. Therefore, the non-orthogonal code set is called TDMA Overloaded on CDMA (ToC) codes [6]. Figure 2 shows the encoding/decoding of two OCI codes for a spreading code set of N-bit size .

When non-orthogonal codes are added to the orthogonal codes, MAI occurs where the accumulator result at the orthogonal decoder deviates. The equation of the sum value for non-orthogonal encoded data can be written as [6]:

$$S = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + \sum_{j=N}^{2N-2} d_T(j).T(j-N+1) \quad (1)$$

where S is the N-cycle waveform of the adder sum, $d_C(j)$ and $d_T(j)$ are the orthogonal CDMA data bit and the non-orthogonal ToC data bit sent by the j^{th} encoder, respectively, $C_o(j)$ and $T(j-N+1)$ are the orthogonal code and non-orthogonal code assigned to the j^{th} encoder, respectively. The non-orthogonal ToC code $T(i)$ is a single "1" chip asserted at the time slot i. The TDMA part of (1) is the sum of products of TDMA chips and data bits to be encoded by the code. Consequently, The TDMA part of (1) can be considered as a single N-chip code because the TDMA chips exist at exclusive time slots in the code. This N-chip ToC code causes MAI to the data spread by orthogonal codes which is represented by the first half of the equation. To overcome the MAI problem, the first chip of the TDMA MAI code is set to zero ($T(1) = 0$), the remaining $N-1$ chips are determined by the non-orthogonal encoded data. (1) can be rewritten as in [6]:

$$S = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T) \quad (2)$$

where $C_n(d_T)$ is the ToC MAI code as a function of the data encoded by the non-orthogonal TDMA codes. Although the MAI term is added to the accumulated value in the orthogonal

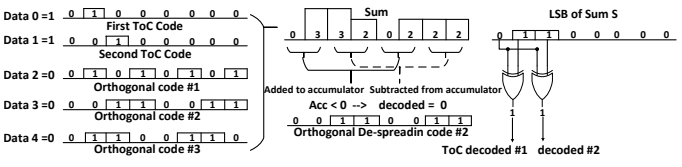

Fig. 2. Encoding and decoding of orthogonal and overloaded codes sharing the CDMA interconnect

code decoders, data encoded with the orthogonal codes can still be decoded properly. Despreading of the k^{th} orthogonal spread data is achieved by multiplying the bus sum by the k^{th} orthogonal spreading code as follows [6]:

$$\begin{aligned} R(k) &= C_o(k).S \\ &= C_o(k)\,(\sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T)\,) \\ &= (-1)^{d_C(j)} N/2 + C_o(k).C_n(d_T) \end{aligned} \quad (3)$$

where $R(k)$ is the correlator decoder output of the k^{th} orthogonal decoder. The first term of (3) represents the autocorrelation term which is equal to $\pm N/2$ according to the data spread by the orthogonal code d_C. The second term of (3) is the correlation between the orthogonal spreading code $C_o(k)$ and the ToC MAI code $C_n(d_T)$. In a balanced orthogonal code, the number of "1" chips is equal to the number of "0" chips and equals to $N/2$. The MAI code is correlated with the orthogonal code at the decoder, therefore, the maximum MAI value contributed by the second term is $\pm N/2$. The MAI term can only reach its maximum value of $\pm N/2$ when the ToC MAI code is the same as the spreading code $C_o(k)$ or its complement $\overline{C_o(k)}$. The sign bit of the accumulated value enables proper decoding of orthogonal data as long as the MAI magnitude $|C_o(k).C_n(d_T)| < N/2$. If the MAI term reaches its maximum value, the correlation result is equal to zero. The zero correlation only occurs in one of two cases, ($d_C = 0$ and $C_n(d_T) = \overline{C_o(k)}$) or ($d_C = 1$ and $C_n(d_T) = C_o(k)$). However, because the first chip of the ToC MAI code $C_n(d_T)$ is set to zero, due to our design of the TOC non-orthogonal codes, the first case never occurs because all Walsh orthogonal codes start with a "0" chip. Therefore, the zero correlation result always indicates that the orthogonal data encoded is "1".

To decode data encoded in the non-orthogonal ToC codes, the even difference property of the CDMA sum is exploited. A two-input XOR gate is used as a decoder in order to check the parity between consecutive CDMA sum values. The two inputs to the XOR gate are the Least-Significant-Bit (LSB) of the CDMA sum at the first clock cycle and the LSB of the CDMA sum at the clock cycle where the "1" chip is inserted in the non-orthogonal code. These two LSB values are stored in a flip-flop during their corresponding clock cycles. The XOR gate output determines the modulus two parity of the difference between the CDMA sum values and, consequently, determines the non-orthogonal encoded data.

Although the number of adder inputs is $2(N-1)$, which is the number of encoders, the number of the adder output bits of the CDMA adder is $m = \log_2 N + 1$ because only N inputs can be "1" at the same clock cycle, the number of ones in the $N-1$ orthogonal inputs are up to $N-1$ while only one non-orthogonal ToC input can be "1" at a given clock cycle. Therefore, the overloaded CDMA scheme adds only one wire to the CDMA adder output although the adder has twice the number of input ports than the conventional CDMA scheme. The aforementioned explanation justifies the significant increase in the OCI capacity with a minimal overhead.

IV. OCNoC Central Router Architecture

In this section, the high-level architecture of the Overloaded CDMA-based NoC central dynamic router (OCNoC)

is advanced. A total of 32 Processing Elements (PEs) are connected by the OCNoC router via 32 network nodes as shown in Figure 3. The router employs a Walsh spreading code set of N-chip length; due to overloading the channel, the number of usable spreading codes is raised to $2(N-1) = 14$. This indicates that the maximum number of packets that can be simultaneously transferred through the router every time is 14. The assignment of spreading codes to transmit nodes is dynamic, meaning that the router assigns spreading codes to network nodes when there is a request from the network node to transmit a packet. Since the 8-bit Walsh code is employed, the packet transfer latency via the router is 8 clock cycles only.

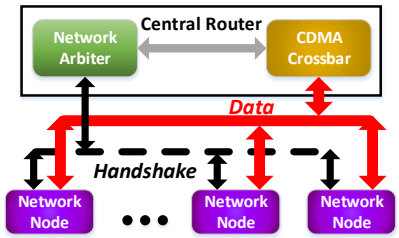

Fig. 3. OCNoC central router network

An alternative to dynamic code assignment is static assignment where each transmit PE is assigned a static spreading code even if it does not need to send packets which may cause under-utilization of the NoC resources. If a conventional CDMA crossbar with static code assignment was used, the central router would need 32-bit length spreading codes to connect 31 PEs while needing 32 clock cycles for data encoding-decoding which is equal to the packet transfer latency. On the other hand, if an overloaded CDMA crossbar with static code assignment is employed, the router would need 16-bit length spreading codes to connect 30 PEs and it would take 16 clock cycles for data encoding-decoding. Therefore, the choice of 8-bit Walsh codes reduces the latency of the CDMA interconnect but only $2(N-1)$ CDMA codes can be used simultaneously, indicating that only 14 packets can be simultaneously transferred through the router. The dynamic code assignment, however, can cause blocking due to the limited number of simultaneous packets transferred dictated by the available spreading codes. Blocking occurs when the number of requests exceeds the number of available spreading codes, or when the receive queues of network nodes are overflowed with incoming packets. However, the blocking problem in the second case can be mitigated by expanding the router queues.

The packet structure of the OCNoC router is divided into 16 bits for the payload and 10 bits for the header to facilitate the conversion from packets to flits for lightweight 16 and 32-bit PEs in our future work. Another motivation for this choice is to compare the achieved improvement with the work of Halak et. al [10] which uses a 16-bit payload width as well. A store and forward switching technique is adopted in the OCNoC router where the packet is not divided into flits, packets are allowed to pass through the router if the transmit request is granted and the destination node's FIFO is not full. Five bits from the header are used as the destination address while the other five bits represent the source address because five bits are needed to address the 32 network nodes. The channel width is 26-bits, where the header and the payload are transmitted by the router to the destination nodes.

Two flavors of the OCNoC router are implemented, an OCNoC router with Serial encoding-decoding (SOCNoC), and OCNoC router with Parallel encoding-decoding (POCNoC). The central router portrayed in Figure 3 consists of three major blocks: the network nodes, the network arbiter, and the CDMA crossbar whose architectures are detailed in this section.

A. CDMA Crossbar

The CDMA crossbar is the main interconnect fabric of the router. The crossbar encodes packets from the network nodes by the codes assigned to them by the arbiter. The encoded packets from each node are then added together and the sum is sent to each network node. The SOCNoC and POCNoC crossbars are depicted in Figure 4 and 5, respectively; where the XOR and AND gate encoders and CDMA adder are replicated $N = 8$ times for the parallel crossbar. The $CWN[i]$ assigned by the arbiter to the port i is passed to the code pool to select the spreading code assigned to each encoder. The same CWN is assigned to the decoders at the destination nodes by the arbiter, thus, encoder-decoder pairs are assigned the same spreading code. Therefore, the CDMA spreading codes are used to route packets by assigning the same CWN to the interconnected encoder-decoder pair. Thus, physical packet switching in the OCNoC router is achieved via code assignment instead of shared time slots and dedicated physical link assignments in TDMA and SDMA crossbars, respectively.

B. Network Node

The network node is the interface of the processing element (PE) to the central router as it transfers packets between the PE and the CDMA crossbar, it is composed of three blocks:

- **FIFO buffers:** The network node contains a transmit and a receive FIFO buffer, each is four-element deep and the element is 26-bit width. The buffer width and depth are generics and can be adjusted at the synthesis time to achieve a different area-latency profile. The transmit FIFO holds packets to be sent from the PE to another PE in the network. The receive FIFO stores packets received from the crossbar.
- **CDMA decoder**: The SOCNoC employs the serial CDMA decoder architecture illustrated in Figure 6. The decoder

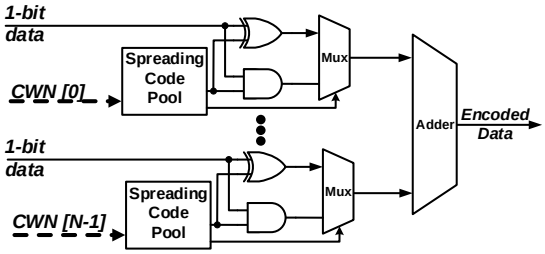

Fig. 4. OCNoC serial CDMA crossbar transmitter [6]

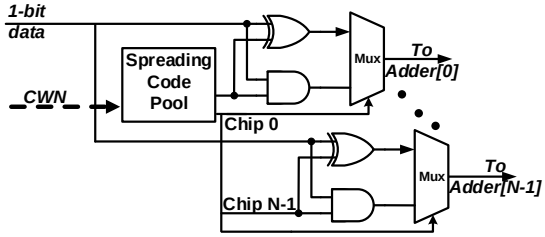

Fig. 5. OCNoC parallel CDMA crossbar transmitter [6]

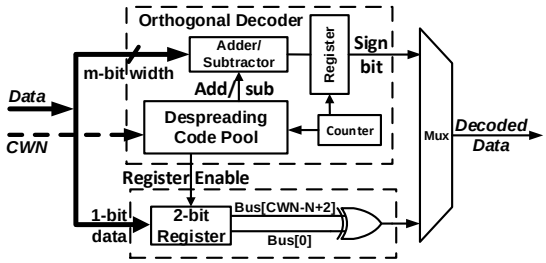

Fig. 6. OCNoC node serial decoder [6]

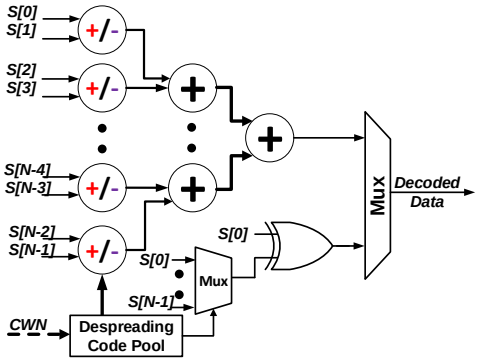

Fig. 7. OCNoC node parallel decoder [6]

contains one serial orthogonal decoder and one overloaded decoder, the decoded packet is selected by a multiplexer from the two decoders according to the spreading code. A Code Word Number CWN from the arbiter is passed to the despreading code pool to select the proper despreading code to be used by the decoder. The parallel CDMA decoder of Figure 7, on the other hand, is employed in the POCNoC router. The orthogonal decoder is implemented using a parallel adder/subtractor controlled by the spreading code chip values. For the overloaded decoders, there is no need for flip-flops to hold the consecutive CDMA sum values because all of the sums are available concurrently.

- **Interface controller**: The interface controller controls the network node operation. The functionality of the network interface is described by the following tasks:
  - If the PE needs to transmit a packet and the transmit FIFO buffer is not full, a write request is issued to the transmit FIFO buffer, and a grant signal is issued to the PE.
  - If the transmit FIFO buffer is not empty, a router access request is issued to the network arbiter.
  - If a router grant is received from the network arbiter, a read request is issued to the transmit FIFO buffer and a buffer element is read by the OCNOC crossbar.
  - If there is a transmit request from the network arbiter which indicates that another node needs to send a packet to the PE and the receive FIFO buffer is not full, then a node grant signal is issued to the arbiter.
  - If the receive FIFO buffer is not empty and the PE is ready to receive, a read request is issued to the receive FIFO buffer and a buffer element is read by the PE.

C. Network Arbiter

The network arbiter controls packet switching by granting network access requests and issuing node access requests. The flow chart of the network arbiter is depicted in Figure 8. Network access requests indicate that a PE has to send a packet to another PE. This request is issued by the network

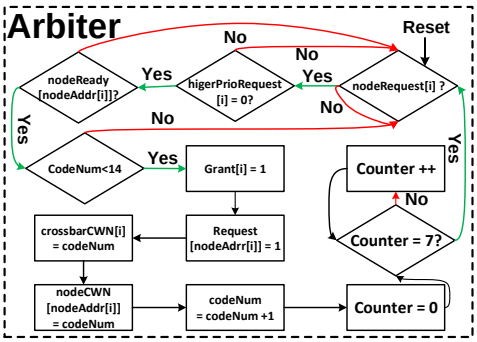

Fig. 8. the OCNOC network arbiter flow chart

nodes and is granted by the network arbiter. When a network access request is issued by a network node to send packets to a destination node, the arbiter issues a node access request to the destination node which asserts a router grant signal if the receive FIFO of the node is not full.

The 14 available codes are assigned by the arbiter to higher priority requests. For each of the 32 network nodes, the arbiter checks if there is a network access request from the node, then checks the number of higher priority requests for that network node. For each network node, the number of higher priority requests is the number of nodes of higher priority that issued an access request to the same PE. This can be expressed as:

$$HPR[i] = \sum_{k=0}^{i-1} R[k] \,\&\, (Addr[k] == Addr[i]) \qquad (4)$$

where $HPR[i]$ is the Higher Priority Request of node i, $R[k]$ is the access request of node k, $Addr[k]$ is the destination address from the network node k, and $\&$ is the logic AND. The $HPR[i]$ must be zero to assert the grant to the requesting node. The HPR method assures that the 14 higher priority nodes only are assigned the available 14 spreading codes. In addition, the $node[Addr[i]]$—the destination node of the packet from node i—must be ready to receive a packet, *i.e.* its receive FIFO is not full. Finally, to assert the grant signal to the $node[i]$, there must be at least one available spreading code.

If all conditions are met, a grant is asserted to the $node[i]$ and a request signal is asserted to the destination node $node[Addr[i]]$. A CWN which indicates the code word number and ranges from 0 to 13 is passed to both the CDMA crossbar and destination node $node[Addr[i]]$. Blocking occurs in three cases: first, if the number of concurrent requests is greater than the number of spreading codes, only packets from higher priority nodes are carried through the CDMA crossbar while packets from other network nodes are queued in the transmit FIFOs; second, when more than two packets have the same destination, only the packet from a higher priority node is allowed to pass while the other packets are queued; third, when the receive FIFO of a destination node is full, a packet from a source node can not be transmitted to it regardless of the availability of spreading codes. Implementing longer queues by increasing the depth of the FIFOs does not reduce the latency incurred by the first two scenarios, but can reduce the latency due to the third one.

V. OCNoC Implementation and Evaluation

Both OCNoC central router variants are synthesized on the 65 *nm* ASIC standard cell library. In this section, the

throughput, area, and energy results of the OCNoC routers are presented and compared to the conventional CDMA NoCs developed in [10]. In [10], the presented NoC is a dynamic CDMA-based central router network where 14 PEs are interconnected with a conventional CDMA crossbar with 8-bit length Walsh codes. Two variants of the router are developed in [10], a Dynamic Serial (DS) CDMA router and a dynamic parallel (DP) CDMA router which are synthesized using the same 65 *nm* technology. Both variants employ 7 orthogonal 8-bit Walsh codes to interconnect 14 PEs. A comparison with a mesh-based NoC architecture from [10] is also provided.

A. Latency and Throughput

The latency of the compared architectures is measured through a Verilog testbench on the ModelSim simulator. Two operation scenarios are tested for the SOCNoC and POCNoC architectures. In the first scenario, each PE sends a single 256-bit message to another PE. All PEs initiate the message transfer at the same clock cycle. The Data Packet Latency (DPL) as a function of the injection load is measured. The DPL is the number of clock cycles between the availability of a packet at a PE for transmission and the arrival of that packet at its intended destination PE. The injection load is the percentage of PEs requesting to transmit a packet during the same cycle.

The latency versus injection load curves are depicted in Figure 9. For the same scenario and spreading code length of $N = 8$, the OCNoC results are compared to the dynamic CDMA NoC results presented in [10] where the injection load is calculated for 14 nodes only. Since the OCNoC router is designed to support 32 nodes, the Halaks work [10] results are interpolated to 32 nodes to establish a fair comparison. The sharp knees in the latency curves of the SOCNoC at injection loads of 46% and 90% in Figure 9 is due to that the number of injected packets is larger than an integer multiples of 14 (the available spreading codes); the OCNoC router latency increases due to the lack of enough codes. The serial CDMA architectures exhibit larger latencies than the parallel ones because data spreading takes N clock cycles. The latency of the SOCNoC architecture is 35.9% less than that of the DS at the highest injection load while the latency of the POCNoC is less than that of the DP by 36.2% at the highest injection load. This improvement in latency is due to the higher capacity provided by the overloaded codes; as the injection load increases, the OCNoC router incurs less blocking due to the overloaded codes which decreases its latency. The latency of the POCNoC is 56.6% less than that of the mesh-based NoC due to the concurrent transmission of the encoded spreading codes, while the SOCNoC has 221% higher latency due to the serial transmission nature of the crossbar.

In the second scenario, a random data traffic pattern is simulated. To compare with [10], only 14 PEs out of 32 are allowed to send packets to any destination PE. A variation in the DPL appears due to the difference in the priority level between PEs and due to the limited number of CDMA codes. Table I shows a comparison between the mean, standard deviation, and deviation to mean ratio of the DPL in clock cycles of the OCNoC solutions to the dynamic CDMA NoC [10]. The mean latencies of the SOCNoC and POCNoC are 102.5% higher and 85.5% lower than that of the DS and DP, respectively, because of the difference in the number of arbitration cycles between

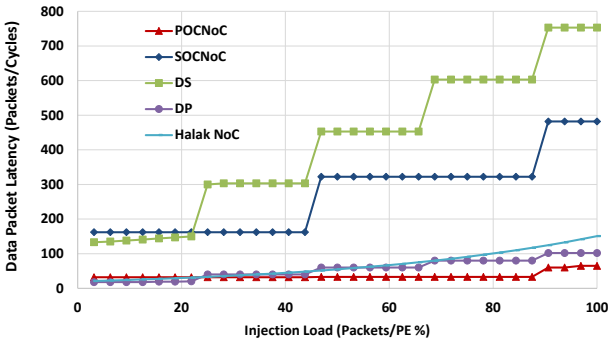

Fig. 9. Data packet latency (DPL) in clock cycles vs the injection load

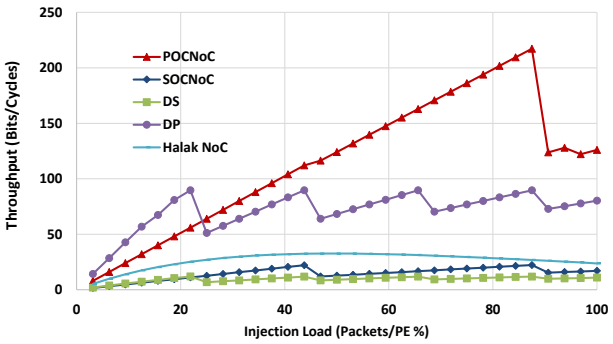

Fig. 10. Throughput in bits per cycle vs the injection load

the two methods. The ASIC maximum clock frequency of the SOCNoC and POCNoC routers are 780 MHz, which results in a worst case latency of 412 *ns* and 43.5 *ns* for the SOCNoC and the POCNoC, respectively, under the presented scenario.

TABLE I. LATENCY OF THE NETWORKS UNDER DYNAMIC TRAFFIC IN CLOCK CYCLES

Network	Mean latency	Standard deviation	Deviation %
SOCNoC	183.4	44.5	24.3
POCNOC	32	0.5	1.7
DS [10]	162	21	12
DP [10]	22	2.7	12
Mesh-based NoC [10]	64	20	30

The OCNoC throughput can be calculated as follows:

$$\Theta = \frac{packet\ size \times number\ of\ packets}{latency} \quad (5)$$

Figure 10 shows the throughput of the OCNoC routers versus the CDMA NoCs of [10]. At the highest injection load, the throughput of the SOCNoC is higher than that of the DS by 56% and the throughput of the POCNoC is higher than that of the DP by 56.9%. Additionally, at an injection load of 87.5%, the SOCNoC and the POCNoC achieve their peak throughput improvement of 82% and 142% over the DS and DP, respectively. The sharp dips in the throughput curves at injection loads of 46% and 90% are due to the sharp rise in the latencies at the same points.

B. Area and Energy Dissipation

Synopsis Design Compiler is employed in the synthesis of the design and the estimation of the area using the 65 nm standard cell library. The area results of the OCNoC routers and CDMA routers of [10] is presented in Table II. The total areas of the SOCNoC and the POCNoC are higher than that of

the DS and DP because the OCNoC routers connect 32 PEs as opposed to 14 PEs in DS and DP routers. However, the area normalized to the number of connected PEs (area/PE) ofthe SOCNoC and POCNoC are 11.8% and 62% less than that of DS and DP, respectively, due to doubling of the number of network nodes and the minimal overhead added by overloaded CDMA. SOCNoC and POCNoC require 62% and 61% less silicon area, respectively, than that of the mesh-based NoC.

TABLE II. AREA OF THE OCNOC AND OTHER CDMA ROUTERS SYNTHESIZED USING 65 nm ASIC STANDARD CELLS

Network	Total area in μm^2	Area per PE in μm^2	Overhead ratio to Mesh-based NoC
SOCNoC	316384.9	9887	-62 %
POCNOC	325132.5	10160.4	-61 %
DS [10]	157038	11217	-57%
DP [10]	377916	26994	3.4%
Mesh-based NoC [10]	365464	26104	0%

Energy figures including the internal and dynamic energy dissipated per cycle in pJ are obtained for the OCNoC routers and compared to the CDMA routers of [10]. Modelsim simulator is used to estimate the switching factors of each architecture which are passed to Synopsys Design Compiler to estimate the dynamic energy. The dissipated energy is estimated for the transmission of a single 256-bit message and the results are depicted in in Table III. The SOCNoC dissipates 75% less internal energy per PE than the DS due to the reduced hardware complexity, in addition to a 70% decrease in dynamic energy dissipation. The internal energy dissipation per PE of the POCNoC is 89.5% less than the DP with an 81.5% reduction in dynamic energy dissipation. POCNoC dissipates 72.5% less internal energy than the mesh-based NoC and 78.6% less dynamic energy dissipation. On the other hand, the SOCNoC router dissipates 70% less internal energy than the mesh-based NoC and 69.2% less dynamic energy consumption.

TABLE III. ENERGY DISSIPATION IN PJ OF THE ASIC OCNOC ROUTER COMPARED TO OTHER ARCHITECTURES

Network	Internal energy (pJ)	Energy per PE (pJ)	Dynamic energy to transfer a message (256 bits) (pJ)
SOCNoC	39.9	1.2	7.2
POCNOC	34.9	1.1	5
DS [10]	67.8	4.8	24.01
DP [10]	147.3	10.5	27.1
Mesh-based NoC [10]	56.2	4	23.4

The two OCNoC variants are implemented and validated on a Xilinx Virtex-7 VC709 FPGA, the resource utilization is depicted in Table IV. It is clear that the crossbar utilizes less than 12% of the total FPGA area.

TABLE IV. AREA OF THE OCNOC ROUTERS ON VIRTEX-7 FPGA

Network	LUTs	Registers	LUT utilization %	FF utilization %
SOC-NoC	18744	12597	4	1
POC-NOC	46788	7040	11	1

VI. CONCLUSIONS

In this paper, we presented the Overloaded CDMA Network On Chip (OCNoC) central router with dynamic code assignment. Overloaded CDMA enables increasing the physical layer capacity of the conventional CDMA crossbar by 100% without increasing the physical layer complexity and latency. Consequently, the OCNoC router can transmit twice the number of packets at the same transfer latency of NoCs employing the conventional CDMA codes. Dynamic code assignment enables the network router to utilize a fixed number of spreading codes regardless of the number of interconnected PEs. Two OCNoC variants were developed, Serial-OCNoC (SOCNoC) and Parallel-OCNoC (POCNoC).

The OCNoC router is compared to existing CDMA-based routers in terms of latency, throughput, area, and energy dissipation. The overloaded CDMA codes reduce the packet blocking induced by dynamic code assignment, which reduces the packet transfer latency. The OCNoC routers provide up to 142% throughput improvement due to the crossbar capacity improvement, with up to 61% and 81.5% area per PE and dynamic energy dissipation reduction, respectively. The deviation in the latency of the presented OCNoC router is down to 1.7% of the mean latency only, which makes the OCNoC a preferred choice for applications requiring guaranteed, high-throughput QoS. Future work includes exploring further architectural optimizations and implementing a higher scale OCNoC-based network with wormhole switching and guaranteed QoS.

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