Overloaded CDMA Crossbar for Network-On-Chip

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***Abstract*— On-chip interconnects are the performance bottleneck in modern system-on-chips. Code-division multiple access (CDMA) has been proposed to implement on-chip crossbars due to its fixed latency, reduced arbitration overhead, and higher bandwidth. In CDMA, medium sharing is enabled in the code space by assigning a limited number of *N*-chip length orthogonal spreading codes to the processing elements sharing the interconnect. In this paper, we advance overloaded CDMA interconnect (OCI) to enhance the capacity of CDMA network-on-chip (NoC) crossbars by increasing the number of usable spreading codes. Serial and parallel OCI architecture variants are presented to adhere to different area, delay, and power requirements. Compared with the conventional CDMA crossbar, on a Xilinx Artix-7 AC701 FPGA kit, the serial OCI crossbar achieves 100% higher bandwidth, 31% less resource utilization, and 45% power saving, while the parallel OCI crossbar achieves *N* times higher bandwidth compared with the serial OCI crossbar at the expense of increased area and power consumption. A 65-node OCI-based star NoC is implemented, evaluated, and compared with an equivalent space division multiple access based torus NoC for various synthetic traffic patterns. The evaluation results in terms of the resource utilization and throughput highlight the OCI as a promising technology to implement the physical layer of NoC routers.**

***Index Terms*— Code-division multiple access (CDMA) interconnect, CDMA router, network-on-chip (NoC), NoC physical layer, overloaded CDMA crossbar.**

I. Introduction

ON-CHIP communications profoundly impact the overall area, performance, and power consumption of modern system-on-chips (SoCs). Increasing the communication overhead degrades the speedup achieved by parallel computing according to Amdahl's law [1]. Therefore, developing efficient high-performance on-chip interconnects has been of paramount importance for the parallel and high-performance computing technologies. Networks-on-chips (NoCs) are the most scalable interconnection paradigm that is capable of addressing various application needs and meet different performance requirements of heavy workloads [2], including latency via adaptive routing [3], throughput via improved path diversity [4], power dissipation by optimizing the NoC to targeted workloads [5], and flexibility by run-time configuration [6].

In NoCs, data are treated as packets, while on-chip processing elements (PEs) are considered as network nodes interconnected via routers and switches. NoCs provide a scalable solution for large SoCs, but they exhibit increased power consumption and large resource overheads [7]. The NoC layering model splits the transaction into four layers: 1) application; 2) transport; 3) network; and 4) physical layers [8]. A crossbar is the basic building block of the NoC physical layer. A crossbar switch is a shared communication medium adopting a multiple access technique to enable physical packet exchange. The main resource sharing techniques adopted by existing NoC crossbars are time-division multiple access (TDMA), where the physical link is time shared between the interconnected PEs [9], and space-division multiple access (SDMA), where a dedicated link is established between every pair of interconnected PEs [10]. The physical layer of an NoC router also contains buffering and storage devices [7].

Code-division multiple access (CDMA) is another medium sharing technique that leverages the code space to enable simultaneous medium access. In CDMA channels, each transmit–receive (TX-RX) pair is assigned a unique bipolar spreading code and data spread from all transmitters are summed in an additive communication channel. The spreading codes in classical CDMA systems are orthogonal—cross correlation between orthogonal codes is zero—which enables the CDMA receiver to properly decode the received sum via a correlator decoder. Classical CDMA systems rely on Walsh–Hadamard orthogonal codes to enable medium sharing. CDMA has been proposed as an on-chip interconnect sharing technique for both bus and NoC interconnect architectures [11]. Many advantages of using CDMA for on-chip interconnects include reduced power consumption, fixed communication latency, and reduced system complexity [12]. A CDMA switch has less wiring complexity than an SDMA crossbar and less arbitration overhead than a TDMA switch, and thus provides a good compromise of both. However, only basic features of the CDMA technology have been explored in the on-chip interconnect literature.

Overloaded CDMA is a well-known medium access technique deployed in wireless communications where the number of users sharing the communication channel is boosted by increasing the number of usable spreading codes at the expense of increasing multiple-access interference (MAI) [13]. The overloaded CDMA concept can be applied to on-chip interconnects to increase the interconnect capacity.

In our previous works, we applied the overloaded CDMA concept to CDMA-based on-chip buses and presented two approaches, namely, MAI-based and difference-based overloaded CDMA interconnects, to increase the bus capacity by %25 and 50%, respectively [14], [15] In this paper, we apply the overloaded CDMA concept to NoCs and advance a novel overloaded CDMA interconnect (OCI) crossbar architecture

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to increase the CDMA router capacity by 100% at marginal cost. Crossbar overloading relies on exploiting special properties of the used orthogonal spreading code set, namely, Walsh–Hadamard codes, to add a set of nonorthogonal spreading codes that can be uniquely identified on the receiver side.

The contributions of this paper are as follows.

1) Introduce two novel approaches that can be deployed in CDMA NoC crossbars to increase the router capacity and, consequently, bandwidth by 100% at marginal cost.
2) Present the OCI mathematical foundations, spreading code generation procedures, and OCI-based router architectures.
3) Develop and evaluate the OCI-based routers built on a Xilinx Artix-7 AC701 evaluation kit and using a 65-nm ASIC technology for several synthetic traffic patterns and compare their latency, bandwidth, and power consumption with the basic CDMA and SDMA switching topologies.

The rest of this paper is organized as follows. The work related to on-chip CDMA interconnects is presented in Section II. Preliminaries of overloaded CDMA in wireless communications, the classical CDMA crossbar architecture, and on-chip CDMA mathematical foundations are introduced in Section III. Fundamentals and mathematical foundations of the OCI code design, serial and parallel OCI crossbar architectures and building blocks, and complexity analysis of the OCI crossbar switches are described in Section IV. The performance evaluation and a comparative analysis of the OCI crossbar switches and OCI-based NoCs are advanced in Section V. Conclusions and future work are portrayed in Section VI.

II. Related Work

Using CDMA as a medium access scheme in crossbar switches provides favorable qualities like the fixed transaction latency and low arbitration overhead. Nikolic *et al.* [16] have proposed a scalable CDMA-based peripheral bus to decrease the number of parallel transfer lines and point-to-point (PTP) buses and to avoid the overhead of TDMA arbiters. This approach reduces the pin count when used at the interface of multiple peripherals to multiple PEs since the data from the peripherals are added and transmitted on fewer lines. The increase in the transaction latency due to data spreading is acceptable because peripherals usually operate at lower frequencies than the master PEs. A master–slave bus wrapper has been presented in [17] and [18], where the data are bundled and spread using orthogonal CDMA codes to decrease the number of parallel transfer lines. The control signals are not encoded to facilitate interconnection to other TDMA buses.

Another CDMA bus implementation has been compared with a TDMA split transaction bus in [11]. The results show that the CDMA bus outperforms the split transaction bus as the number of PEs increases since the CDMA bus avoids bus contention and queuing delays, which hinder the scalability of a TDMA bus. A multilevel 2-bit CDMA bus has been utilized in [19] as an input/output (I/O) reconfiguration scheme that also demonstrates a reduction in the bus contention over the TDMA bus. CDMA and TDMA have been combined in the CT-Bus where data are multiplexed over both the time and code domains [12]. The CT-Bus depicts that the communication overhead of CDMA is lower than that of TDMA as the CDMA bus controller is required to assign only spreading codes, while the TDMA controller must perform arbitration every clock cycle. The CT-Bus performance surpasses its TDMA counterpart for heterogeneous traffic since it combines the TDMA bus scalability with the CDMA channel continuity.

A CDMA-based NoC has been compared with a PTP bidirectional ring-based NoC in [20], and the comparison shows that the CDMA NoC's fixed data transfer latency is equal to the best case latency of the PTP of the same channel width. The fixed data transfer latency of the CDMA NoC is attributed to concurrent interconnect sharing by the network nodes. A hierarchical CDMA star NoC router has been presented in [21] and [22]. The CDMA router is connected in a star–star topology and a star-mesh topology and compared with pure mesh and fat tree topologies. The CDMA star NoC demonstrates fewer resources and routing complexity than its rivals. The maximum hop count of the CDMA star NoC router is lower than that of the compared topologies due to the concurrent transmission of packets through the router. The CDMA interconnect topology presented in [21] and [22] is made scalable either by doubling the number of chips in the Walsh code set to double the number of ports that can be connected to the router or by using more routers in a star or mesh fashion. The CDMA encoding and decoding operations are local to the router, and therefore, the same Walsh codes can be reused in each NoC router.

A CDMA-based multicast switch has been employed in a 2-D mesh NoC in [23]. The CDMA-based switch allows simultaneous packet transmission due to code-space multiplexing. This approach reduces the hop count in multicasting schemes and allows packets to reach the destination PEs simultaneously, which is preferred in real-time applications. A 14-node CDMA-based network has been developed in [24]. The assignment of spreading codes to TX-RX pairs is dynamic based on the request from each node. Two architectures have been introduced in the CDMA-based network: a serial CDMA network, where each data chip in the spreading code is sent in one clock cycle, and a parallel CDMA network, where all data chips are sent in the same cycle. The CDMA-based serial and parallel networks have been compared with a conventional CDMA network, a mesh-based NoC, and a TDMA bus. For the same network area, the bandwidth of the parallel CDMA network is higher than the throughput of the mesh-based NoC and the TDMA bus due to the simultaneous medium access nature of CDMA.

Standard basis codes are proposed as a replacement to Walsh CDMA codes in [25]. Standard basis codes resemble the TDMA signaling scheme because each code consists of only a single chip of one and the remaining chips are zeros. The orthogonality of TDMA codes is attributed to that the phase shift of the one chip is an integer number of the code duration indicating that the cross correlation between various codes is zero. The orthogonality of TDMA codes enables them to replace the Walsh codes as spreading and despreading CDMA

codes, which reduces the complexity of the channel adder and decoder as the maximum sum of the TDMA codes is one.

Most related works proposing CDMA for on-chip interconnects investigate only architectural and topological enhancements of the basic wireless spread spectrum CDMA scheme. In this paper, a different aspect of the CDMA technology for on-chip interconnects is addressed, which is increasing the interconnect capacity by applying overloaded CDMA to the existing on-chip CDMA-based NoC routers. To the best of our knowledge, we are the first group to investigate this specific point in this paper and its precedings [14], [15].

III. Preliminaries

In this section, overloaded CDMA in wireless communications and the requirements of its on-chip interconnect counterpart and preliminaries of the classical on-chip CDMA switch presented by Nikolic *et al.* [16] are presented.

A. Overloaded CDMA in Wireless Communications

Direct sequence spread spectrum CDMA (DSSS-CDMA) is a leading approach for medium sharing in wireless communications where a set of orthogonal spreading codes composed of a stream of chips of length N are multiplied by the transmitted data bits such that each data bit is spread in N cycles [26, Ch. 2]. A unique spreading code is assigned to every TX-RX pair sharing the communication channel. Data streams of users sharing the channel are spread and simultaneously transmitted to an additive communication channel. Despreading is achieved by applying the correlation operation to the received sum, where each receiver can extract its data by correlating it with the assigned spreading code. Orthogonality between spreading codes guarantees unique identification of every code received in the channel sum by exploiting the associative and distributive properties of the addition operation carried out by the communication channel. In wireless communications, random effects such as noise, fading, and multipath arising in the communication channel affect proper identification of the received sum, which increases the bit error rate (BER) of the received data.

Unfortunately, the number of orthogonal codes in a spreading code set is usually limited to the spreading code length N, which reduces the channel utilization efficiency. Overloaded CDMA has been proposed in the wireless communication literature to increase the number of spreading codes by adding nonorthogonal codes that can be identified on the receiver side [13]. Increasing the channel utilization comes at the expense of relaxing the orthogonality requirements of the spreading codes and increasing MAI, which consequently increases the BER. The proposed overloaded CDMA spreading codes in wireless communications are accompanied with complicated receiver structures making use of multiuser detection instead of the simple correlator or matched filter receiver employed in basic DSSS-CDMA.

In this paper, we apply the overloaded CDMA concepts developed in the wireless communication field to on-chip interconnects to increase the CDMA-based NoC capacity. However, on-chip interconnects are significantly different from wireless communication channels on both the characteristic and requirement levels. In the following, basic features of overloaded CDMA will be enumerated from the on-chip interconnect perspective to sum up the OCI design considerations.

1) Overloaded CDMA is a medium access technique deployed in wireless communications based on DSSS-CDMA.
2) The complexity of wireless overloaded CDMA limits its applicability for on-chip interconnects, which require simple communication schemes to meet the performance requirements.
3) Despite that wireless CDMA is usually adopted in conjunction with other modulation techniques, only baseband binary CDMA is considered for on-chip interconnects, which can be directly implemented in digital platforms such as FPGAs.
4) Because only digital on-chip interconnects are considered, random effects arising in analog communication channels such as noise, fading, and MAI can be efficiently mitigated using error detection and correction techniques [27]. Therefore, such random effects are neglected in this paper.
5) Consequently, due to the last two assumptions, the complexity of the CDMA receivers can be significantly reduced to fit the on-chip interconnect requirements.

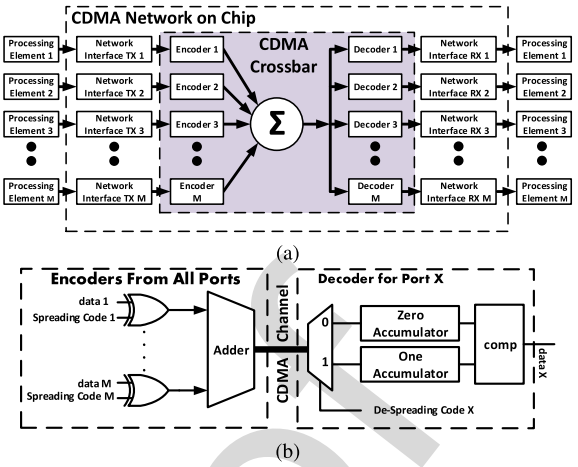

Fig. 1. (a) CDMA NoC router architecture. (b) Classical CDMA crossbar.

B. Classical CDMA Crossbar Switch

Fig. 1(a) illustrates the high-level architecture of a CDMA-based NoC router. The physical layer of the router is based on the classical CDMA switch presented by Nikolic *et al.* [16] and illustrated in Fig. 1(b). The switch is composed of a number of XOR encoders, a channel adder, and accumulator-based decoders. In the encoder, an N-chip length binary orthogonal code, generated from a Walsh spreading code set, is XORed with the transmitted data bit and sent out serially, indicating that a single bit is spread in a duration of N clock cycles. Therefore, the crossbar transaction frequency f_t and operating clock frequency f_c are related as $f_t = f_c/N$. The number of TX-RX ports sharing the CDMA router equals

$M = N - 1$ for Walsh spreading codes. Serial streams from all transmit PEs sharing the crossbar are added together and the binary sum is sent to a decoding circuit feeding the receiving ports. Binary encoding and signaling are preferred over multilevel signaling for implementing the channel adder due to its superior performance, reliability, and its inherent support by digital platforms. The data sent over the CDMA crossbar switch are given by the following equation:

$$S(i) = \sum_{j=1}^{M} d(j) \oplus C_o(j, i) \tag{1}$$

where $S(i)$ is an m-bit binary number representing the channel sum at the ith clock cycle, the crossbar width $m = \lceil \log_2 M \rceil$, $d(j)$ is the data bit from the jth encoder, $C_o(j, i)$ is the ith chip of the jth orthogonal spreading code, and $\oplus$ is the XOR operation. In the ordinary CDMA crossbar, the adder has $M = N - 1$ input bits and $m = \lceil \log_2 M \rceil = log_2 N$ output bits.

The decoder is implemented as a wrapper that cross correlates the serialized channel sum with the signature code assigned to the TX-RX pair. The decoding process is periodic and the decoding cycle lasts for N clock cycles. The despreading operation is realized using a correlator decoder that correlates the received channel sum with the spreading code assigned to the TX-RX pair. As the spreading codes are generated from the bipolar Walsh code family, the correlation process mainly involves two operations: multiplying the received sum by ± 1 according to the spreading code and accumulation. However, multiplication can degrade the router's performance. Fortunately, the spreading codes are bipolar—composed of only (± 1) chips—eliminating the need for the expensive multiplication operation and reducing it to simple addition and subtraction operations.

Two accumulators are used to realize the correlator decoder. According to the assigned CDMA code, the received sum is passed to the zero accumulator when the current chip value is "0" and to the one accumulator when the chip value is "1," which is equivalent to multiplying the crossbar sum by ± 1. At the uth decoder and ith cycle, the inputs to the zero and one accumulators ($\text{In}_z(i)$ and $\text{In}_o(i)$) are given by

$$\text{In}_z(i) = \overline{C_o(u, i)} \cdot S(i), \quad \text{In}_o(i) = C_o(u, i) \cdot S(i) \tag{2}$$

where $C_o(u, i)$ is the despreading chip of the uth decoder.

The one and zero accumulator circuits accumulate their inputs during the decoding cycle and are reset to zero at the end of each decoding cycle. The values held by the zero and one accumulators are given by the following equations:

$$\text{Acc}_z = \sum_{i=1, i \neq j}^{N} \text{In}_z(i), \quad \text{Acc}_o = \sum_{j=1, j \neq i}^{N} \text{In}_o(i) \tag{3}$$

where $0 < i, j \leq N$ and the indexes i and j do not take the same value for both Acc_z and Acc_o.

Consequently, each accumulator adds $N/2$ different inputs during the decoding cycle because the spreading codes are balanced—the number of zeroes equals the number of ones in a balanced code. At the end of the decoding cycle, the decoder has received the sum of spreading codes or their complements encoded according to the data spread by the transmit ports. Decoding the crossbar sum containing an orthogonal code or its complement using other orthogonal codes (cross-correlation) results in adding the same value to both accumulators. Decoding the crossbar sum containing an orthogonal code or its complement using the same code (autocorrelation) makes the value of one accumulator greater than the other accumulator by the number of ones in the code, which equals $N/2$ for balanced spreading codes. The cross correlation between orthogonal codes yields zero, while autocorrelation (multiplying the code by itself or its complement) yields $\pm N/2$. Therefore, the difference between the one and zero accumulators is always $\pm N/2$ for orthogonal spreading codes. This can be directly derived for the accumulator decoder using the correlation definition and Walsh code orthogonal property. For bipolar Walsh codes, the CDMA sum can be written as

$$S = \sum_{j=1}^{M} (-1)^{d(j)} C_o(j) \tag{4}$$

where S is the N-cycle waveform of the crossbar sum, $d(j)$ are the data sent by the jth user, and $C_o(j)$ is the orthogonal code assigned to user j. The decoding operation at the kth receiver is achieved by correlating the crossbar sum by the kth spreading code as follows:

$$R(k) = C_o(k) \cdot S = C_o(k) \cdot \sum_{j=1}^{M} (-1)^{d(j)} C_o(j)$$

$$= \sum_{j=1}^{M} (-1)^{d(j)} C_o(j) \cdot C_o(k) = (-1)^{d(j)} C_o(k) \cdot C_o(k)$$

$$+ \sum_{j=1, j \neq k}^{M} (-1)^{d(j)} C_o(j) \cdot C_o(k) = (-1)^{d(j)} N/2 \tag{5}$$

where $R(k)$ is the correlator output of the kth decoder, $M = N - 1$ for orthogonal Walsh codes, the autocorrelation term $C_o(k) \cdot C_o(k)$ yields $N/2$ for a balanced binary spreading code of length N, and the cross-correlation term $C_o(k) \cdot C_o(j)$ yields zero for any orthogonal spreading codes with different $k \neq j$. At the end of the decoding cycle, the difference between the two accumulators is always $N/2$ in the MAI- and noise-free crossbar, e.g., for $N = 8$, the difference between the two accumulators is 4. Comparing the two accumulators directly indicates the encoded data via the sign of $R(k)$; if the zero accumulator's content is greater than the one accumulator's content, the sent data bit is "1"; otherwise, the bit is "0." Therefore, the correlation operation can directly determine the encoded data without errors due to neglecting random effects. The main advantage of the accumulator decoder is replacing the multiplication-based correlator with an addition-based one.

IV. Overloaded CDMA Interconnect

Fig. 1(a) illustrates the high-level architecture of the CDMA-based NoC router. The CDMA router has M transmit/receive ports. The main difference between the overloaded

and classical CDMA routers is that $M > N-1$ for the former due to channel overloading. Each PE is connected to two network interfaces (NIs), transmit and receive NI modules. During packet transmission from a PE, the packet is divided into flits to be stored in the transmit NI first-input first-output (FIFO). The router arbiter then selects M winning flits at most from the top of the NI FIFOs to be transmitted during the current transaction. The selected flits must all have an exclusive destination address to prevent conflicts, and a winner from two conflicting flits is selected according to the router's priority scheme. The employed priority scheme is the fixed winner that takes all priority schemes; only one of the transmitters is given a spreading code and is acknowledged to start encoding. Once done, the router assigns CDMA codes to each transmit and receive NI. NIs with empty FIFOs or conflicting destinations are assigned all-zero CDMA codes such that they do not contribute MAI to the CDMA channel sum. Afterward, flits from each NI are spread by the CDMA codes in the encoder module.

The data are spread into N chips, where N is the CDMA code length that equals the number of clock cycles in a single crossbar transaction. Spread data chips from all encoders are summed by the CDMA crossbar adder and the sum is sent out serially to all decoders. The encoding/decoding process lasts for N clock cycles synchronized via a counter. At each decoder, the assigned code is cross correlated with the received sum to decode the data from the summed chips. The decoded flits are stored in the receive NI FIFOs until they are read by the PEs. In this paper, we focus on the high-level architecture and implementation details of the overloaded CDMA crossbar represented by the gray block in Fig. 1(a).

A store and forward flow control and a deterministic routing algorithm are employed in the OCI router. The routing algorithm lies at the network layer, which is a higher layer than the physical layer containing the crossbar switch. According to the OSI model design principles, each layer of the model exists as an independent layer. Theoretically, one can substitute one protocol for another at any given layer without affecting the operation of layers above or below. Thus, using the same flow control protocol and routing algorithm enables comparing the OCI-based router with SDMA- and TDMA-based routers.

A. OCI Crossbar High-Level Architecture

The main objective of this paper is increasing the number of ports sharing the ordinary CDMA crossbar presented in [17], while keeping the system complexity unchanged using simple encoding circuitry and relying on the accumulator decoder with minimal changes. To achieve this goal, some modifications to the classical CDMA crossbar are advanced. Fig. 2 depicts the high-level architecture of the OCI crossbar for a single-bit interconnection. The same architecture is replicated for a multibit CDMA router. M TX-RX ports share the CDMA router, where spread data from the transmit ports are added using an arithmetic binary adder having M binary inputs and an m-bit output, where $m = \lceil \log_2 M \rceil$. The adder is implemented in both the reference and pipelined architectures. A controller block is used for code assignment and arbitration tasks. Each PE is interfaced to an encoder/decoder wrapper enabling data spreading/despreading.

Unlike orthogonal spreading codes, which are XORed with the binary data bit, an AND gate is utilized to spread data using nonorthogonal spreading codes. The AND gate encoder works as follows: if the transmitted data bit is "0," it sends a stream of zeros during the whole spreading cycle, which does not cause MAI on the channel; if the transmitted data bit is "1," the encoder sends a nonorthogonal spreading code. Therefore, the additional MAI spreading code will either contribute an MAI value of one or zero each clock cycle because the encoder is an AND gate. The XOR encoder of the ordinary CDMA crossbar cannot be used to encode the OCI codes because it only complements the spreading code chips, so an XOR gate will cause MAI to the crossbar whether the data bit is "0" or "1." A hybrid encoder is developed for both orthogonal and nonorthogonal spreading with an XOR gate, an AND gate, and a multiplexer unit, as shown in Fig. 2. Two decoder types are implemented for orthogonal and nonorthogonal data. More details about each component of the OCI crossbar will be presented in Section IV-C after describing the OCI code design procedures and decoding scheme in Section IV-B.

B. OCI Code Design

The Walsh–Hadamard spreading code family has a featured property that enables CDMA interconnect overloading. The difference between any consecutive channel sums of data spread by the orthogonal spreading codes for an odd number of TX-RX pairs M is always even, regardless of the spread data. This property means that for the $N-1$ TX-RX pairs using the Walsh orthogonal codes, one can encode additional $N-1$ data bits in consecutive differences between the N chips composing the orthogonal code. Thus, exploiting this property enables adding 100% nonorthogonal spreading codes, which can double the capacity of the ordinary CDMA crossbar. In this section, the code design methodology, mathematical foundations, and the decoding details of both T-OCI and P-OCI codes are provided. The notations used throughout this paper are listed in Table I.

An AND gate encoder is used to encode data with nonorthogonal spreading codes as shown in Fig. 2(a). Therefore, for a nonorthogonal encoder, if data to transmit are one, a single spreading chip at a specific time slot in the spreading cycle is added to the channel sum, which causes the consecutive sum difference to deviate. The nonorthogonal codes imitate the TDMA signaling scheme as each code is composed of a single chip of "1" sent in a specific time slot. The encoding/decoding scheme presented in this paper provide a novel approach that enables coexistence between CDMA and TDMA signals in the same shared medium. Therefore, the developed encoder is called TDMA overloaded on CDMA interconnect (T-OCI). Fig. 3 shows an encoding/decoding example of two T-OCI codes for a spreading code of length $N = 8$. An odd number of orthogonal codes must be used simultaneously to preserve the even difference property of Walsh codes.

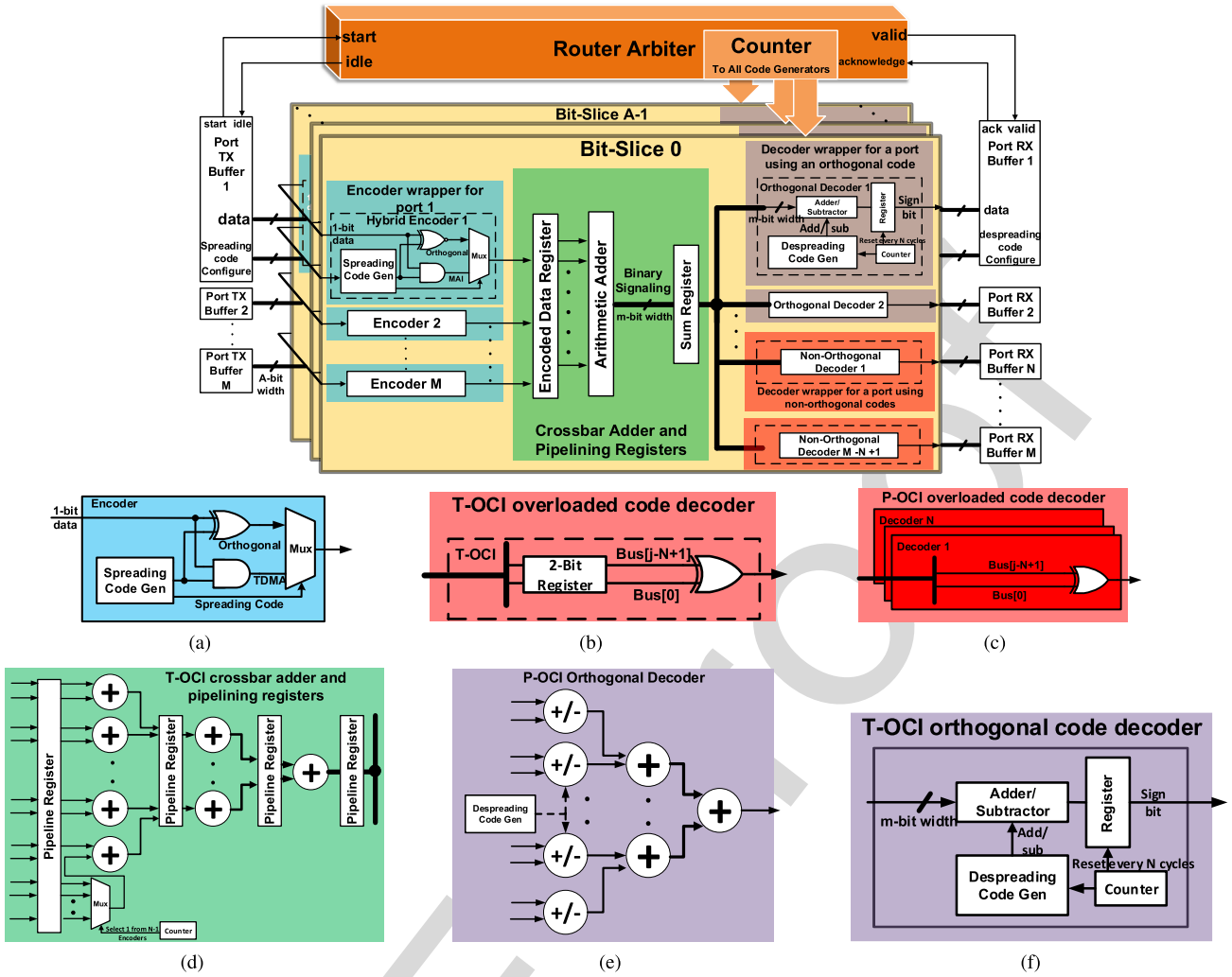

Fig. 2. High-level architecture and building blocks of the OCI crossbar. (a) T-OCI/P-OCI hybrid encoder. (b) T-OCI nonorthogonal decoder. (c) P-OCI nonorthogonal decoder. (d) T-OCI pipelined crossbar tree adder, in which the adder is replicated N times for P-OCI crossbar. (e) P-OCI orthogonal decoder. (f) T-OCI orthogonal decoder.

TABLE I
DEFINITION OF NOTATIONS

Notation	Description
N	Orthogonal spreading code Length
M	Number interconnected ports
m	Number of crossbar adder wires
S	Sum of CDMA chips carried by the channel
d_C	Data bit encoded by an orthogonal CDMA code
d_T	Data bit encoded by a non-orthogonal TDMA code
$C_o(j)$	The j^{th} chip of the orthogonal CDMA code
$T(j)$	The j^{th} chip of the non-orthogonal TDMA code
C_n	TDMA MAI code (non-orthogonal spread data)
$R(k)$	Output of the k^{th} correlator decoder

TDMA codes cause MAI to the sum of CDMA spread data. The equation of the crossbar sum for both CDMA and TDMA encoded data can be written as

$$S = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + \sum_{j=N+1}^{2N-1} d_T(j) \cdot T(j-N+1) \quad (6)$$

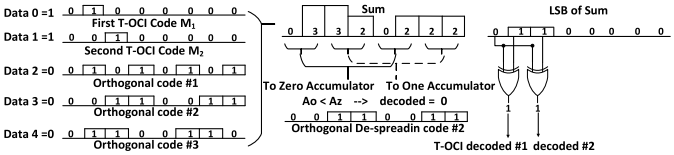

Fig. 3. Encoding/decoding of three orthogonal codes and two T-OCI codes.

where S is the N-cycle waveform of the channel sum, $d_C(j)$ is the orthogonal CDMA data bit sent by the jth user, $d_T(j)$ is the nonorthogonal TDMA data bit sent by the jth, $C_o(j)$ is the orthogonal code assigned to the jth user, and $T(j-N+1)$ is the TDMA code assigned to the jth user. The TDMA code $T(i)$ is a single chip of "1" assigned at the ith time slot. The TDMA term of the equation is the sum of products of TDMA chips and their corresponding data bits. This term can be viewed as another N-chip spreading code added to the orthogonal spread data represented by the first term of the equation. It should be indicated that the first chip of the TDMA MAI code is always set to zero ($T(1) = 0$), and the remaining $N-1$ chips are assigned according to the encoded data bits;

this note is the key to properly decode both orthogonal and nonorthogonal spread data. Equation (6) can be rewritten as follows:

$$S = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T) \tag{7}$$

where $C_n(d_T)$ is the TDMA MAI code as a function of the nonorthogonal data. The number of the crossbar adder output bits is $m = \log_2 N + 1$ despite that the number of adder inputs is $2(N-1)$, which is the total number of orthogonal and nonorthogonal TX-RX pairs sharing the OCI crossbar. This is because at any time instance, there can be only N inputs having a value of "1" in the T-OCI encoding scheme. The number of the adder output bits is specifically important because it directly determines the crossbar wiring density.

Orthogonal spread data can be still decoded properly using the accumulator-based correlator. Despreading of the kth orthogonal spread data is achieved by multiplying the crossbar sum by the kth orthogonal spreading code as follows:

$$\begin{aligned} R(k) &= C_o(k) \cdot S = C_o(k) \left(\sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T) \right) \\ &= (-1)^{d_C(j)} N/2 + C_o(k) \cdot C_n(d_T). \end{aligned} \tag{8}$$

The first term of (8) is the autocorrelation term, which is equal to $\pm N/2$ according to the data spread d_C, while the second term is the cross correlation between the orthogonal spreading code $C_o(k)$ and the nonorthogonal MAI TDMA code $C_n(d_T)$. The maximum MAI value contributed by the second term is $\pm N/2$ because the MAI code is correlated with a balanced orthogonal code, where the number of "1" chips is equal to the number of "0" chips and equals $N/2$. This case can only occur if the MAI TDMA code constructed by the nonorthogonal encoded data is identical to $C_o(k)$ or its complement $\overline{C_o(k)}$, which yields $\pm N/2$, respectively.

As long as the MAI magnitude $|C_o(k).C_n(d_T)| < N/2$, the nonzero correlation result will always facilitate proper decoding of the orthogonal data, where the comparator circuit can still be used to detect the accumulator sign. The main challenge is decoding orthogonal data when the MAI TDMA code is identical to the spreading code or its complement, which might cause the correlation result to be zero. Zero correlation indicates either cases of [$d_C = 0$ and $C_n(d_T) = \overline{C_o(k)}$] or [$d_C = 1$ and $C_n(d_T) = C_o(k)$]. However, because the first chip of the MAI TDMA code $C_n(d_T)$ is always forced to zero, the first case can be excluded because all Walsh orthogonal spreading codes start with "0." Therefore, the zero correlation result always indicates that the orthogonal data encoded is "1."

On the other hand, decoding nonorthogonal TDMA data can be achieved by exploiting the even difference property of the Walsh orthogonal codes. Because the T-OCI decoding is achieved by parity checking the difference between consecutive crossbar sums, a two-input XOR gate is used. The XOR gate inputs are the current least significant bit (LSB) of the crossbar sum and the LSB of the crossbar sum corresponding to the first chip of the Walsh codes stored in a flip-flop (FF)

$$d_T(j) = S(0) \oplus S(j - N + 1). \tag{9}$$

The XOR gate output determines the parity of the difference, and consequently, the nonorthogonal TDMA encoded data.

The P-OCI crossbar employs the same Walsh and Overloaded Codes as the T-OCI crossbar; however, the data spreading and decoding are parallelized. Instead of using one XOR gate to encode the data bit using the spreading code, N XOR gates are used where the data bit is XORed with the N chips of the spreading code in parallel. The nonorthogonal AND gate encoders are also replicated N times. Since the N chips are available in parallel in the same clock cycle, N replicas of the crossbar adder are necessary to add the N chips from each transmit port. Therefore, the encoding and decoding equations governing P-OCI are the same as those of the T-OCI.

C. OCI Crossbar Building Blocks

Two variants are realized for each OCI crossbar, reference and pipelined architectures. The pipelined architecture is implemented to increase the crossbar operating frequency, and consequently, bandwidth by adding nonfunctional pipelining registers to reduce the crossbar critical path. The OCI crossbar shown in Fig. 2 is basically composed of three main building blocks: 1) the encoder wrappers; 2) the decoder wrappers; and 3) the crossbar adder blocks, which are described in the following.

1) *Crossbar Controller:* At the beginning of each crossbar transaction, the controller assigns spreading codes to different encoders. The assignment of orthogonal despreading codes to receive ports is fixed, i.e., does not change between the crossbar transactions. Therefore, for a router port to initiate the communication with the receive port it addresses, its encoder must be assigned a spreading code that matches the destined decoder. If two different ports request to address the same decoder, the controller allows one access and suspends the other according to a predefined arbitration scheme. This code assignment scheme is called receiver-based protocol [20]. In this paper, a static allocation scheme that allocates fixed spreading codes to all encoders is used. To interconnect a large number of PEs, a torus, star, or hybrid NoC topology can be realized where the assignment of spreading codes is local to each router. Consequently, each new packet arriving at a router is assigned a spreading code corresponding to its exit port decoder. The crossbar controller issues handshake signals to the transmit and receive ports with matching spreading codes to enable the transmitter encoders and receiver decoders.
2) *Hybrid Encoder:* The encoder is hybrid, it can encode both orthogonal and nonorthogonal data. A transmitted data bit is XORed/ANDed with the spreading code to produce the orthogonal/nonorthogonal spread data, respectively. A multiplexer chooses between the orthogonal and nonorthogonal inputs according to the code type assigned to the encoder as depicted by Fig. 2(a). The encoder is replicated N times for the P-OCI crossbar.

TABLE II

COMPLEXITY ANALYSIS OF THE CONVENTIONAL CDMA AND OCI CROSSBARS FOR N-CHIP SPREADING CODES (FOR A GENERIC NUMBER OF PORTS $2(N-1)$); BOLD NUMBERS BETWEEN BRACKETS ARE NUMERICAL VALUES COMPUTED FOR $N = 8$ AS AN ILLUSTRATIVE EXAMPLE

Topology	Instances	Crossbar Wires	Encoders	Orthogonal Decoders		Non-orthogonal decoders		Counters
		FF	COMB	FF	COMB	FF	COMB	
Conventional CDMA Crossbar	Encoders: $N-1$ **(7)**, Orthogonal decoders: $N-1$ **(7)**	$\lceil log_2(N) \rceil$ **(3)**	1-AND	$\lceil log_2((N/4)*(N-1)) \rceil$ **(4)**	Adder output width: $(\lceil log_2((N/4)*(N-1)) \rceil)$ **(4)**	0	0	Adder wires: $\lceil log_2(N) \rceil$ **(3)**
T-OCI Crossbar	Encoders: $2(N-1)$ **(14)**, Orthogonal decoders: $N-1$ **(7)**, T-OCI Decoders: $N-1$ **(7)**	$\lceil log_2(N+1) \rceil$ **(4)**	1-AND, 1-XOR, 1-MUX	$\lceil log_2((N/4)*(N-1)) \rceil + 1$ **(5)**	Adder output width: $(\lceil log_2((N/4)*(N-1)) \rceil + 1)$-bit **(5)**	2	1-XOR	FFs: $\lceil log_2(N) \rceil$ **(3)**
P-OCI Crossbar	Encoders: $2N(N-1)$ **(112)**, Orthogonal decoders: $N-1$ **(7)**, T-OCI Decoders: $N-1$ **(7)**	$N\lceil log_2(N+1) \rceil$ **(4)**	N-AND, N-XOR, N-MUX	0	Adders: $\sum_{i=0}^{log_2 N-1} (log_2 N - i)$ **(6)**	0	1-XOR	

3) *Crossbar Adder:* For a spreading code set of length N, the number of crossbar TX-RX ports is equal to $M = 2(N-1)$. In the T-OCI crossbar, sending a "1" chip to the adder is mutually exclusive between nonorthogonal transmit ports according to the T-OCI encoding scheme. This indicates that among the $2(N-1)$ inputs to the adder, there are guaranteed $(N-2)$ zeros, while the maximum number of "1" chips is N. Therefore, a multiplexer is instantiated to select only a single input of the nonorthogonal TDMA encoded data bits and discard the remaining bits that are guaranteed to be "0." Thus, the adder has only N-bit inputs, $N-1$ from orthogonal encoders, and 1 from the multiplexer, as shown in Fig. 2(d). The sum produced by the adder circuit needs ($\log_2 N$) wires. The number of needed stages of registers to pipeline the adder is ($\log_2 N$), as depicted in Fig. 2(d). N replicas of the crossbar adder are instantiated for the parallel encoding adopted in the P-OCI crossbar.
4) *Custom Decoder:* There are four decoder types for different CDMA decoding techniques: the orthogonal T-OCI and P-OCI decoders and the overloaded T-OCI and P-OCI decoders. The orthogonal T-OCI decoder is an accumulator implementation of the correlator receiver. $N-1$ accumulator decoders are instantiated in all CDMA crossbar types for orthogonal data despreading. Instead of implementing two different accumulators (the zero and one accumulator), an up–down accumulator is implemented and the accumulated result is the difference between the two accumulators of the conventional CDMA decoder as shown in Fig. 2(f). The accumulator adds or subtracts the crossbar sum values according to the despreading code chip and resets every N cycles. The sign bit of the accumulated value directly indicates the decoded data bit, where the positive sign is decoded as "1," while the negative sign is decoded as "0." The P-OCI orthogonal decoder shown in Fig. 2(e) differs from the T-OCI orthogonal decoder in receiving the adder sum values concurrently not sequentially; therefore, the accumulator loop is unrolled into a parallel adder.

The T-OCI overloaded decoder depicted in Fig. 2(b) is composed of a 2-bit register to store the LSBs of two sum values, first of which is $S(0)$ and the second is $S(j-N+1)$, where j is the number of the T-OCI decoders ($N \leq j \leq 2N-2$). The two bits are fed to the XOR gate, which decodes nonorthogonal spread data. The T-OCI decoder is replicated N times to implement the P-OCI decoder of Fig. 2(c). The 2-bit register is not needed anymore because the $S(0)$ and $S(j-N+1)$ values exist in the same cycle. The T-OCI and P-OCI crossbar architectures contain $(N-1)$ orthogonal decoders and $(N-1)$ overloaded decoders.

Table II provides a comprehensive complexity analysis of the OCI crossbars compared with that of the classical CDMA crossbar as a function of the spreading code length N. The complexity of all crossbar components is analyzed and expressed in terms of the number of FFs and combinational logic (COMB). Some crossbar components like the counter can be replicated M times, one replica is used in each decoder. However, the number of such replicated components can be reduced if different decoders can share one replica. Therefore, there is a tradeoff between resource sharing, which reduces resource utilization but increases the wiring density and resource replication. For the orthogonal CDMA decoder, the maximum number of ones the accumulator can add at any decoding cycle is $(N-1)$ ones ("1" from each encoder). The accumulator adds the received crossbar sum up for $N/2$ cycles and subtracts it for $N/2$ cycles, due to the balanced nature of the Walsh orthogonal codes. During any $N/2$ cycles, there only exists $N/4$ "1" chips in each of the $N-1$ codes due to the orthogonality property. Therefore, the value stored in the accumulator never exceeds $N(N-1)/4$ for orthogonal codes only. Thus, the accumulator and its pipelining register are $\lceil log_2(N(N-1)/4) \rceil$ wide. For the OCI decoder, an additional bit is added to the accumulator output due to increasing the maximum sum value by 1.

For the same number of chips N, the conventional CDMA and T-OCI crossbar variants exhibit the same latency, which is N clock cycles because a single data bit is spread in N chips. The latency of the P-OCI crossbar, however, is only one cycle. The conventional CDMA crossbar utilizes the least area, while the P-OCI crossbar utilizes the largest area due to the additional $N-1$ hybrid encoders and $N-1$ XOR decoders per spreading chip. However, the area normalized to the number of ports in the T-OCI crossbar is lower than

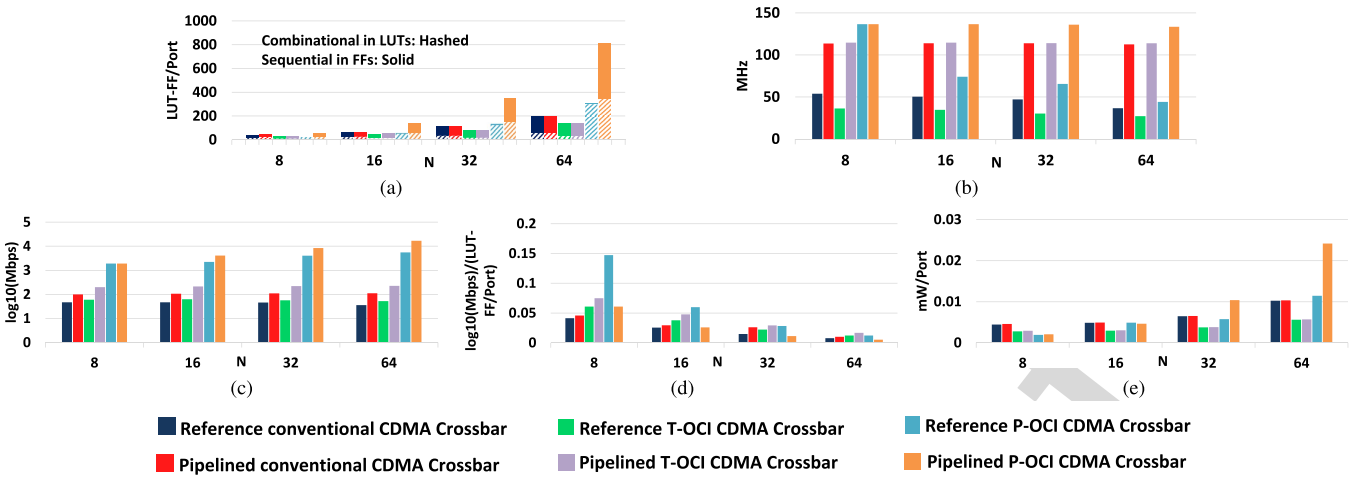

Fig. 4. Implementation results of the OCI crossbars for a spreading code length $N = \{8, 16, 32, 64\}$. (a) Resources as combinational (hashed bars) and noncombinational (solid bars) in LUT-FF/port. (b) Maximum clock frequency f_c in megahertz. (c) Log-scaled crossbar bandwidth BW in megabits per second. (d) Dynamic power dissipated P_D in milliwatts per port. (e) Dynamic power dissipated P_D in mw/port

that in the conventional CDMA crossbar. The P-OCI crossbar bandwidth, however, is the highest of the three crossbars. The T-OCI crossbar bandwidth is double that of the conventional CDMA crossbar because the number of interconnected ports is doubled, while the P-OCI bandwidth is $N \times 100\%$ higher than that of the T-OCI crossbar. Therefore, the P-OCI crossbar has the highest bandwidth at the expense of higher complexity, while the conventional CDMA crossbar has the lowest bandwidth and complexity and the T-OCI crossbar seizes the middle ground in terms of area and bandwidth.

V. Performance Evaluation

In this section, the performance evaluation results of the developed OCI crossbars are presented.

A. OCI Crossbar Evaluation

In this section, a comparison among the conventional CDMA, T-OCI, and the P-OCI crossbars is drawn. A crossbar containing a number of TX-RX ports is built with full capacity, i.e., the number of ports is the maximum number offered by the crossbar. All CDMA crossbar architectures in both the reference and pipelined variants are implemented and validated on an Artix-7 AC701 evaluation kit. The developed crossbars are evaluated for different spreading code lengths $N = \{8, 16, 32, 64\}$. To establish a fair comparison among different crossbar architectures with different numbers of ports, all utilization metrics are normalized to the number of crossbar ports M. The evaluation results, including the resource utilization expressed in the number of lookup tables (LUTs) and FFs per port, maximum crossbar frequency, dynamic power consumption per port, and crossbar bandwidth, are illustrated in Fig. 4.

As depicted in Fig. 4(a), for a spreading code of length N, the resource utilization per port of the T-OCI crossbar is lower than that of the ordinary CDMA crossbar by 31%. This salient reduction in the normalized resource utilization is due to the significant increase in the CDMA interconnect capacity compared with the marginal overhead added by the crossbar circuitry. On the other hand, the P-OCI crossbar is 400% larger than the conventional CDMA crossbar due to the parallel crossbar adders. Increasing the spreading code length N increases the resource utilization per port, due to the increasing crossbar complexity. Specifically, with increasing N, the size of the crossbar adder and accumulator decoder circuitry increases. The resource utilization of all crossbar pipelined variants is always larger than that of the basic architectures due to the additional nonarchitectural pipelining registers.

For all reference architectures, the operating frequency is limited by the critical path length of the crossbar adder. For various CDMA crossbars of the same spreading code length N, orthogonal spreading and despreading circuits are identical and nonorthogonal data encoders and decoders are running parallel to the orthogonal spreading circuitry with a shorter critical path length. The input size of the adder circuit is equal to M, the number of transmitting ports, which varies with the CDMA crossbar type. Fig. 4(b) illustrates that for a spreading code of fixed length N, the crossbar frequency of the overloaded CDMA crossbars is lower than the basic CDMA crossbar frequency due to the increase in the adder circuit size. The pipelined architecture splits the adders' critical path into $\lceil \log_2(N+1) \rceil$ stages, which improves the maximum crossbar frequency at the expense of the extra nonarchitectural registers and output latency. The maximum crossbar frequency in the pipelined architectures no longer depends on the adder, yet it depends on the maximum delay of both the adder stage and I/O circuitry. The crossbar frequency decreases with increasing N for both overloaded and ordinary CDMA crossbars due to the increasing computational complexity of the adders, as shown in Fig. 4(b). The clock frequency of the P-OCI crossbar is higher than that of the T-OCI crossbar due to the absence of the highly loaded synchronization counters and some pipelining registers presented in the T-OCI crossbar.

With increasing N, the drop in the maximum clock frequency is compensated for by the increase in the

crossbar bandwidth, due to the capacity enhancement gained by crossbar overloading as shown in Fig. 4(c). The log-scaled crossbar bandwidth is plotted for only a single bit per port interconnected via the CDMA crossbar. For a fixed N, the enhancement of the CDMA crossbar bandwidth for the P-OCI and T-OCI crossbars over the classical CDMA crossbars is salient. Generally, the CDMA crossbar bandwidth BW is given by the following equation:

$$BW = W\ f_c\ \frac{M}{\Gamma} \tag{10}$$

where W is the port width in bits, f_c is the crossbar clock frequency, M is the number of crossbar ports, and Γ is the number of cycles to encode 1 bit of data from all ports. The T-OCI crossbar bandwidth demonstrates a significant increase over the ordinary CDMA crossbar as it has an overloading ratio of $M/N = 2$ compared with the basic CDMA crossbar ratio of $M/N = 1$ for the same $\Gamma = N$ for both crossbars. For the P-OCI crossbar, however, $\Gamma = 1$, and therefore, the bandwidth of the P-OCI crossbar is N times that of the T-OCI crossbar and $2N$ times that of the conventional CDMA crossbar. Fig. 4(d) depicts the bandwidth-to-resource ratio; the T-OCI and P-OCI crossbars offer higher ratios compared with the conventional CDMA crossbar due to the significant bandwidth enhancement compared with the induced marginal resource overhead.

As illustrated in Fig. 4(e), for a spreading code of fixed length N, the dynamic power dissipation per port, estimated by the Xilinx Vivado tool for a single crossbar transaction, is decreased by 45% for the T-OCI crossbar due to the offered capacity enhancement. However, due to the increased area and parallel encoding–decoding of the P-OCI crossbar, its dynamic power dissipation is 133% higher than that of the conventional CDMA crossbar. With increasing N, power dissipation per port increases for all CDMA crossbars due to the increased size and complexity of the crossbar components.

B. OCI Communication Reliability Considerations

Since the OCI scheme relies on adding detectable interference to the interconnect, the robustness of the OCI crossbar to noise may be raised as a concern; would the added MAI reduce the robustness of the OCI compared with that of the conventional CDMA interconnect? According to [27], while full-swing digital implementations have typically been able to assume BER values less than 10^{-15} over the operating range of voltages and frequencies, this assumption does not hold true for custom low-swing interconnect implementations and modern deep submicrometer circuits. Indeed, in wireless communication channels, overloaded CDMA would increase the BER compared with the classical CDMA because of overloading the channel with MAI. Wireless channels are purely analog exposing them to all random effects such as noise. On the other hand, the OCI crossbar adopts binary signaling to carry the crossbar sum instead of multilevel or analog signaling. The binary nature of the OCI interconnect enables enhancing its robustness by employing error detection and correction techniques to mitigate such random effects.

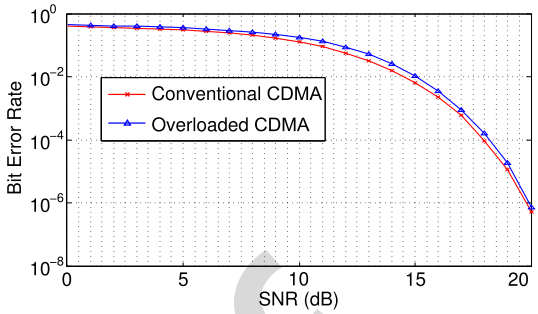

Fig. 5. BER versus SNR of the OCI and conventional CDMA crossbars in the presence of AWGN.

To empirically test the robustness of the OCI crossbar on the FPGA platforms, a testbench was applied for $N = 16$ OCI crossbar implemented on a Zedboard FPGA evaluation kit with a 100-MHz clock frequency and a 1 V core voltage. Zynq's embedded processor runs a program generating 10^6 consecutive crossbar transactions and compares the decoded output with the input data. Zero errors were detected during the experiment, which lasted for 27 h.

On the other hand, to study the reliability of OCI and conventional CDMA links in the presence of error sources such as noise, the BER of the overloaded and classical CDMA links subject to additive white Gaussian noise (AWGN) with a variable signal-to-noise ratio (SNR) was computed using MATLAB simulation for the following test scenario: the CDMA sum S can be expressed as a bit vector $S = [s_1\ s_2\ \ldots\ s_m]$, where $m = \lceil \log_2 M \rceil$. An AWGN vector of size m is added to the sum S to generate the corrupted sum $\tilde{S}$ such that $\tilde{S} = S + [N_1\ N_2\ \ldots\ N_m]$, where each N_i is an AWGN with zero mean and variance $\sigma^2 = \text{Ps/SNR}$, where Ps is the signal power. A total of 10^7 test vectors are randomly generated per SNR value, which changes from 0 to 20. The BER–SNR curves shown in Fig. 5 depicts an increase in the BER of overloaded CDMA compared with that of classical CDMA in a digital communication channel subject to AWGN. The BER increase is no greater than 72% and its average is 35%.

C. OCI for NoCs: Analytical Evaluation

Table III provides an analytical comparison between the OCI crossbars and some existing bus and NoC interconnection techniques. The comparison is established for an interconnect of M TX-RX pairs representing the number of ports in an NoC router. The compared metrics are the interconnect complexity normalized to the port width in bits W, interconnect latency in clock cycles, and the interconnect bandwidth normalized to the crossbar operating frequency f_c and W.

As a bus, the OCI crossbar provides a higher bandwidth than the CDMA peripheral bus [16]. The CDMA peripheral bus interfaces multiple peripherals to multiple PEs on a shared CDMA bus. The OCI technique can be applied to the peripheral bus to increase the number of interconnected PEs and peripherals without degrading the transaction latency. In the CDMA parallel transfer wrapper of [17] and [18],

TABLE III
ANALYTICAL COMPARISON BETWEEN THE T-/P-OCI CROSSBARS AND OTHER INTERCONNECTS

Bus/NoC Topology	Complexity / W	One packet Latency (clock cycles)	$BW/(f_c \times W)$
T-OCI Crossbar	M Hybrid encoders $M/2$ Accumulator decoders $M/2$ XOR decoders	$M/2$	2
P-OCI Crossbar	M^2 Hybrid encoders $M/2$ Accumulator decoders $M/2$ XOR decoders $M/2$ adders	1	$2M$
TDMA-based CDMA NoC [25]	M AND Encoders M Accumulator decoders	M	1
CDMA Peripheral bus [16]	M Encoders M Accumulator decoders	M	1
CDMA Parallel Transfer Wrapper [17], [18]	M Encoders M Accumulator decoders	M	1
CDMA NoC [20]	M Encoders/router M Accumulator decoders	1 hop M per hop	1
PTP NoC [20]	One Bypass multiplexers/router	1 hop (best case) M hops (worst case)	M (best case) $1/M$ (worst case)
CDMA star NoC [22]	M Encoders/router M Accumulator decoders	1 hop (best case) 3 hops (worst case)	*N.A.*
Mesh NoC with CDMA Multicastable Router [23]	M Encoders/router M Accumulator decoders	5 hops worst case in 5×5 mesh	*N.A.*
Mesh NoC without CDMA Multicastable Router [23]	*N.A.*	8 hops worst case in 5×5 mesh	*N.A.*
Parallel Dynamic CDMA NoC [24]	M^2 Encoders/router M Accumulator decoders	1 hop 1 per hop	M
Mesh NoC [28]	M buffers/router $M \times M$ SDMA cross bar/router	1 hop 1	M
MPEG-2 PTP [29]	M ports (wiring)	1	M
MPEG-2 NoC [29]	M buffers/router $M \times M$ SDMA cross bar/router	1 hop 1 per hop	M
MPEG-2 TDMA Bus [29]	M ports (wiring) arbiter	1	1

the number of parallel transfer lines is reduced by bundling data using spreading codes. The OCI spreading codes can be used to bundle more data bits on the same number of wires. Therefore, the OCI crossbar can provide higher bandwidth than the CDMA peripheral bus and the CDMA parallel transfer wrapper of the same complexity due to crossbar overloading.

The CDMA encoding–decoding scheme presented in [25] is based on the standard basis TDMA codes, which replace the orthogonal Walsh codes. The encoders are consequently replaced by an AND gate, the bus adder is reduced to a single XOR gate, the channel wires are reduced to one wire per bit because no two TDMA chips are simultaneously sent in the same clock cycle. This scheme resembles TDMA signaling but adopts the CDMA arbitration procedures where the code assignment is done once every N encoding–decoding bus cycle. On the other hand, our proposed OCI technique enables coexistence between both CDMA and TDMA codes on a single channel, providing double bandwidth, while utilizing less area than two independent TDMA and CDMA crossbars.

The data transfer latency of the CDMA NoC router in [20] is equal to the best case latency of a PTP network. This data transfer latency of the CDMA router can be reduced using fewer chips per spreading code while keeping the number of PEs unchanged through utilizing the OCI technique. The CDMA NoC router in [22] utilizes the orthogonal Walsh code set to interconnect a maximum of N network nodes, where N is the number of chips in a spreading code. The presented

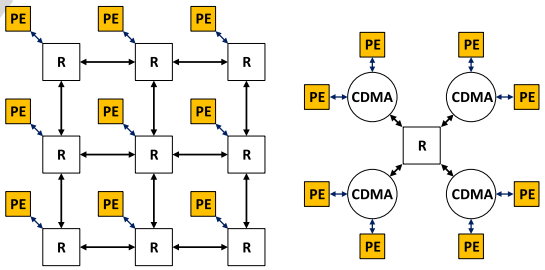

Fig. 6. (a) CONNECT torus topology (b) versus the OCI star topology.

routers can exploit the OCI schemes to double the number of ports of the network router without increasing the spreading code length and hence without increasing the hop latency. The multicast router of [23] interconnects four ports and four PEs. The OCI technique can double the capacity of the switch without increasing the hop latency, and therefore, each PE can multicast more packets through the router in one hop.

The modules of the MPEG-2 encoder in [29] are interconnected using PTP, NoC, and TDMA bus topologies to evaluate these three different interconnects. The NoC is shown to have a close bandwidth to a PTP at fewer logic resources and wiring area and much higher bandwidth than the TDMA bus. The conventional parallel CDMA buses of [24] demonstrate equal bandwidth to the best case bandwidth of mesh NoCs [28], in addition to the fixed latency, due to the simultaneous medium access by the interconnected PEs. The P-OCI crossbar can

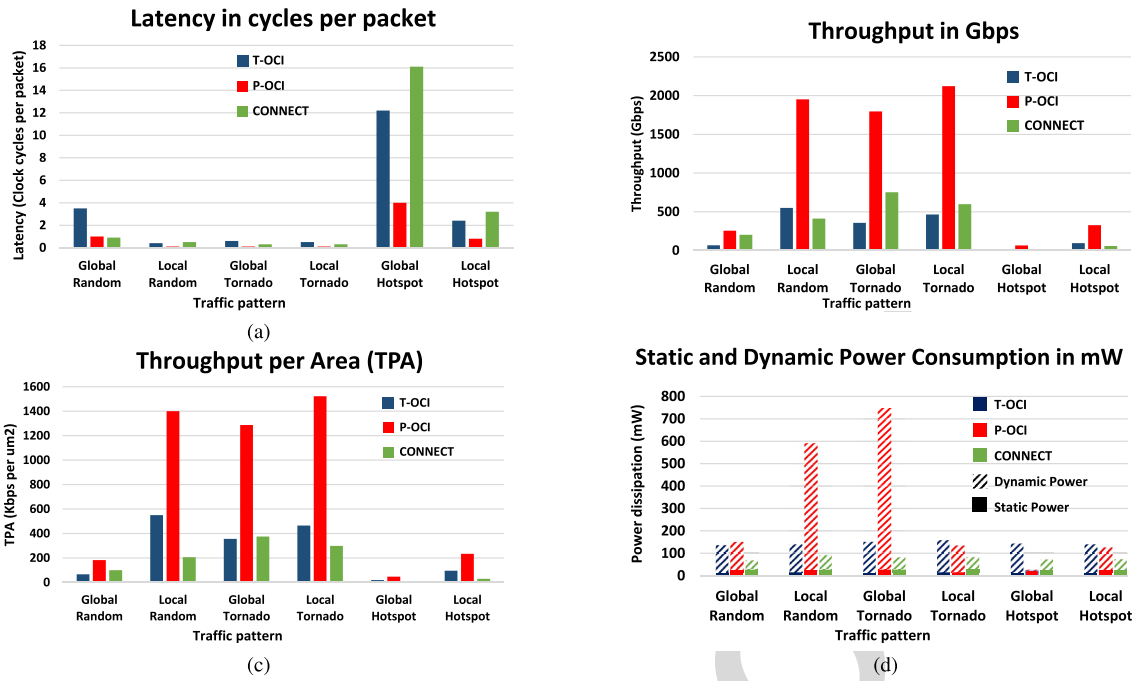

Fig. 7. (a) Latency, (b) throughput, (c) TPA, and (d) power dissipation of T-OCI, P-OCI, and CONNECT NoCs.

provide a higher bandwidth and a lower latency than the conventional parallel CDMA buses by simultaneously transmitting all the N chips of the spreading code in parallel due to overloading. This analytical discussion highlights the OCI capability of substituting the classical CDMA interconnect in any CDMA-based bus or NoC architecture while providing higher bandwidth at the same latency or interconnecting the same number of ports at lower latency per transaction.

D. OCI for NoCs: Experimental Evaluation

To study the effectiveness of the OCI crossbar in a full working NoC, a 65-node star topology is built using five OCI routers, each of the 13 PEs is connected by an OCI router with $N = 8$, and the five OCI routers are interconnected by an SDMA central router. Both T-OCI- and P-OCI-based NoCs are compared with a 64-node, 16-bit flit, and 8-ary 2-cube torus SDMA-based NoC generated by the CONNECT tool [30]. The CONNECT NoC employs simple input queued routers with peek flow control. Fig. 6 illustrates the torus topology employed by the CONNECT NoC versus the star topology adopted by the OCI NoC. The star topology is chosen for the OCI NoC since the improvement of the OCI complexity against the SDMA router increases as the number of ports increases due to the linear increase in the OCI crossbar area compared to the quadratic increase in the SDMA crossbar area. Similarly, the torus topology was chosen for the CONNECT NoC since the torus SDMA crossbars have a low number of ports, which is translated to lower complexity. Since each router in a torus network accommodates five buffers, the buffer spacing offered in the CONNECT NoC is 64×5, while the spacing of the OCI-based NoC is equal to the number of PEs plus the number of buffers in the central router, which equates to $65 + 5$. Therefore, to equalize the buffer spacing in the compared NoCs, the OCI buffer width is sized four times the CONNECT buffer width. Consequently, the flit size of the OCI-based NoC is 64 bits. Table IV lists the implementation results of the three NoCs on the 65-nm ASIC technology, the area of the T-OCI NoC is 45% less than that of the CONNECT NoC, while the area of the P-OCI is 30% less than that of the CONNECT NoC, despite the larger flit size with a reduction in latency due to their lower complexity.

TABLE IV
IMPLEMENTATION RESULTS ON THE ASIC 65-*nm* TECHNOLOGY

	CONNECT	T-OCI	P-OCI
Area (mm^2)	1.998	1.09	1.394
Clock period (ns)	0.72	1.11	1.36

The performance comparisons of the T-OCI and P-OCI NoCs versus the CONNECT NoC are depicted in Fig. 7 for six synthetic traffic patterns and for the same packet width of 256 bits. The uniform, hotspot, and tornado traffic patterns are employed with two variants: local and global traffic. In the global traffic, the traffic pattern is applied to the entire network, while in the local traffic, the traffic pattern is applied to separate clusters. For the OCI network, there are five clusters corresponding to the five OCI routers. On the other hand, the 64 nodes of the torus network are divided in the network layer into five clusters according to the proximity of the routers. The experiment is conducted by subjecting the NoCs to different traffic patterns for 500 clock cycles each, the latency per packet is then computed by dividing the total number of clock cycles (500) by the total number of packets arrived successfully to their target PEs in each traffic pattern.

Additionally, the throughput Θ is calculated as follows:

$$\Theta = \frac{N_c \times N_b \times N_p}{t_c} \quad (11)$$

where N_c is the number of the simulation clock cycles (500), N_b is the number of bits per packet (256), N_p is the number of packets received by the target PEs, and t_c is the clock period.

As illustrated by Fig. 7(a), the latency in clock cycles per packet of the T-OCI is higher than that of the CONNECT NoC in most traffic patterns due to the serial spreading of packets. However, the latency is lower in the hotspot traffic pattern due to the smaller number of hops needed to reach the hotspot node. Additionally, the P-OCI NoC offers lower packet latency compared with the CONNECT NoC for all traffic patterns except for the uniform pattern since torus NoCs are better in balancing the injected load than star NoCs. Consequently, the P-OCI throughput shown in Fig. 7(b) is higher than that of the CONNECT NoC for all traffic patterns due to its lower clock period. Moreover, the improvement in throughput and area of the T-OCI and P-OCI over those of the CONNECT NoC appears in the throughput-to-area ratio (TPA) comparison in Fig. 7(c). However, as illustrated in Fig. 7(d), the dynamic and static power consumption of the OCI-based NoC for all traffic patterns are larger than that of the CONNECT NoC except the uniform pattern despite the P-OCI's higher clock period. Therefore, the improvement in the TPA of the T-OCI and P-OCI routers comes at the expense of increasing power consumption. Resource replication and adapting the clock speed can be employed to enhance the power consumption.

VI. Conclusion

In this paper, we introduced the concept of overloaded CDMA crossbars as the physical layer enabler of NoC routers. In overloaded CDMA, the communication channel is overloaded with nonorthogonal codes to increase the channel capacity. Two crossbar architectures that leverage the overloaded CDMA concept, namely, T-OCI and P-OCI, are advanced to increase the CDMA crossbar capacity by 100% and $2N \times 100\%$, respectively, where N is the spreading code length. We exploited featured properties of the Walsh spreading code family employed in the classical CDMA crossbar to increase the number of router ports sharing the crossbar without altering the simple accumulator decoder architecture of the conventional CDMA crossbar. Generation procedures of nonorthogonal spreading codes are presented along with the reference and pipelined architectures for each crossbar variant. The T-/P-OCI crossbars were implemented and validated on a Xilinx Artix-7 AC701 FPGA evaluation kit.

The performance of the OCI crossbars is compared with that of the conventional CDMA crossbar. The dynamic power is reduced by 45% for the T-OCI crossbar but increased by 133% for the P-OCI crossbar. The T-OCI crossbar utilizes 31% fewer resources, while the P-OCI crossbar uses 400% more resources compared with the conventional CDMA crossbar. The OCI crossbar suitability for NoCs has been established by analytically and experimentally evaluating a fully working OCI-based NoC. A 65-node OCI-based star NoC was realized and compared with an SDMA-based torus NoC generated by CONNECT. The evaluation results demonstrate the superiority of the OCI-based NoCs in terms of area and throughput.

Many future work directions are inspired by this paper including exploiting the mathematical properties of the code space to find additional nonorthogonal codes and boost the CDMA interconnect capacity and exploring more architectural optimizations of the OCI crossbar. Studying the robustness of CDMA interconnects and its enhancement techniques will be one of the prior future research points. Moreover, we plan to investigate using the OCI-based routers in different network topologies, evaluate their performance using standard benchmarks, and study their suitability for various applications.

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Overloaded CDMA Crossbar for Network-On-Chip

Khaled E. Ahmed, *Member, IEEE*, Mohamed R. Rizk, *Senior Member, IEEE*, and Mohammed M. Farag, *Member, IEEE*

***Abstract*— On-chip interconnects are the performance bottleneck in modern system-on-chips. Code-division multiple access (CDMA) has been proposed to implement on-chip crossbars due to its fixed latency, reduced arbitration overhead, and higher bandwidth. In CDMA, medium sharing is enabled in the code space by assigning a limited number of *N*-chip length orthogonal spreading codes to the processing elements sharing the interconnect. In this paper, we advance overloaded CDMA interconnect (OCI) to enhance the capacity of CDMA network-on-chip (NoC) crossbars by increasing the number of usable spreading codes. Serial and parallel OCI architecture variants are presented to adhere to different area, delay, and power requirements. Compared with the conventional CDMA crossbar, on a Xilinx Artix-7 AC701 FPGA kit, the serial OCI crossbar achieves 100% higher bandwidth, 31% less resource utilization, and 45% power saving, while the parallel OCI crossbar achieves *N* times higher bandwidth compared with the serial OCI crossbar at the expense of increased area and power consumption. A 65-node OCI-based star NoC is implemented, evaluated, and compared with an equivalent space division multiple access based torus NoC for various synthetic traffic patterns. The evaluation results in terms of the resource utilization and throughput highlight the OCI as a promising technology to implement the physical layer of NoC routers.**

***Index Terms*— Code-division multiple access (CDMA) interconnect, CDMA router, network-on-chip (NoC), NoC physical layer, overloaded CDMA crossbar.**

I. Introduction

ON-CHIP communications profoundly impact the overall area, performance, and power consumption of modern system-on-chips (SoCs). Increasing the communication overhead degrades the speedup achieved by parallel computing according to Amdahl's law [1]. Therefore, developing efficient high-performance on-chip interconnects has been of paramount importance for the parallel and high-performance computing technologies. Networks-on-chips (NoCs) are the most scalable interconnection paradigm that is capable of addressing various application needs and meet different performance requirements of heavy workloads [2], including latency via adaptive routing [3], throughput via improved path diversity [4], power dissipation by optimizing the NoC to targeted workloads [5], and flexibility by run-time configuration [6].

In NoCs, data are treated as packets, while on-chip processing elements (PEs) are considered as network nodes interconnected via routers and switches. NoCs provide a scalable solution for large SoCs, but they exhibit increased power consumption and large resource overheads [7]. The NoC layering model splits the transaction into four layers: 1) application; 2) transport; 3) network; and 4) physical layers [8]. A crossbar is the basic building block of the NoC physical layer. A crossbar switch is a shared communication medium adopting a multiple access technique to enable physical packet exchange. The main resource sharing techniques adopted by existing NoC crossbars are time-division multiple access (TDMA), where the physical link is time shared between the interconnected PEs [9], and space-division multiple access (SDMA), where a dedicated link is established between every pair of interconnected PEs [10]. The physical layer of an NoC router also contains buffering and storage devices [7].

Code-division multiple access (CDMA) is another medium sharing technique that leverages the code space to enable simultaneous medium access. In CDMA channels, each transmit–receive (TX-RX) pair is assigned a unique bipolar spreading code and data spread from all transmitters are summed in an additive communication channel. The spreading codes in classical CDMA systems are orthogonal—cross correlation between orthogonal codes is zero—which enables the CDMA receiver to properly decode the received sum via a correlator decoder. Classical CDMA systems rely on Walsh–Hadamard orthogonal codes to enable medium sharing. CDMA has been proposed as an on-chip interconnect sharing technique for both bus and NoC interconnect architectures [11]. Many advantages of using CDMA for on-chip interconnects include reduced power consumption, fixed communication latency, and reduced system complexity [12]. A CDMA switch has less wiring complexity than an SDMA crossbar and less arbitration overhead than a TDMA switch, and thus provides a good compromise of both. However, only basic features of the CDMA technology have been explored in the on-chip interconnect literature.

Overloaded CDMA is a well-known medium access technique deployed in wireless communications where the number of users sharing the communication channel is boosted by increasing the number of usable spreading codes at the expense of increasing multiple-access interference (MAI) [13]. The overloaded CDMA concept can be applied to on-chip interconnects to increase the interconnect capacity.

In our previous works, we applied the overloaded CDMA concept to CDMA-based on-chip buses and presented two approaches, namely, MAI-based and difference-based overloaded CDMA interconnects, to increase the bus capacity by %25 and 50%, respectively [14], [15] In this paper, we apply the overloaded CDMA concept to NoCs and advance a novel overloaded CDMA interconnect (OCI) crossbar architecture

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to increase the CDMA router capacity by 100% at marginal cost. Crossbar overloading relies on exploiting special properties of the used orthogonal spreading code set, namely, Walsh–Hadamard codes, to add a set of nonorthogonal spreading codes that can be uniquely identified on the receiver side.

The contributions of this paper are as follows.

1) Introduce two novel approaches that can be deployed in CDMA NoC crossbars to increase the router capacity and, consequently, bandwidth by 100% at marginal cost.
2) Present the OCI mathematical foundations, spreading code generation procedures, and OCI-based router architectures.
3) Develop and evaluate the OCI-based routers built on a Xilinx Artix-7 AC701 evaluation kit and using a 65-nm ASIC technology for several synthetic traffic patterns and compare their latency, bandwidth, and power consumption with the basic CDMA and SDMA switching topologies.

The rest of this paper is organized as follows. The work related to on-chip CDMA interconnects is presented in Section II. Preliminaries of overloaded CDMA in wireless communications, the classical CDMA crossbar architecture, and on-chip CDMA mathematical foundations are introduced in Section III. Fundamentals and mathematical foundations of the OCI code design, serial and parallel OCI crossbar architectures and building blocks, and complexity analysis of the OCI crossbar switches are described in Section IV. The performance evaluation and a comparative analysis of the OCI crossbar switches and OCI-based NoCs are advanced in Section V. Conclusions and future work are portrayed in Section VI.

II. Related Work

Using CDMA as a medium access scheme in crossbar switches provides favorable qualities like the fixed transaction latency and low arbitration overhead. Nikolic *et al.* [16] have proposed a scalable CDMA-based peripheral bus to decrease the number of parallel transfer lines and point-to-point (PTP) buses and to avoid the overhead of TDMA arbiters. This approach reduces the pin count when used at the interface of multiple peripherals to multiple PEs since the data from the peripherals are added and transmitted on fewer lines. The increase in the transaction latency due to data spreading is acceptable because peripherals usually operate at lower frequencies than the master PEs. A master–slave bus wrapper has been presented in [17] and [18], where the data are bundled and spread using orthogonal CDMA codes to decrease the number of parallel transfer lines. The control signals are not encoded to facilitate interconnection to other TDMA buses.

Another CDMA bus implementation has been compared with a TDMA split transaction bus in [11]. The results show that the CDMA bus outperforms the split transaction bus as the number of PEs increases since the CDMA bus avoids bus contention and queuing delays, which hinder the scalability of a TDMA bus. A multilevel 2-bit CDMA bus has been utilized in [19] as an input/output (I/O) reconfiguration scheme that also demonstrates a reduction in the bus contention over the TDMA bus. CDMA and TDMA have been combined in the CT-Bus where data are multiplexed over both the time and code domains [12]. The CT-Bus depicts that the communication overhead of CDMA is lower than that of TDMA as the CDMA bus controller is required to assign only spreading codes, while the TDMA controller must perform arbitration every clock cycle. The CT-Bus performance surpasses its TDMA counterpart for heterogeneous traffic since it combines the TDMA bus scalability with the CDMA channel continuity.

A CDMA-based NoC has been compared with a PTP bidirectional ring-based NoC in [20], and the comparison shows that the CDMA NoC's fixed data transfer latency is equal to the best case latency of the PTP of the same channel width. The fixed data transfer latency of the CDMA NoC is attributed to concurrent interconnect sharing by the network nodes. A hierarchical CDMA star NoC router has been presented in [21] and [22]. The CDMA router is connected in a star–star topology and a star-mesh topology and compared with pure mesh and fat tree topologies. The CDMA star NoC demonstrates fewer resources and routing complexity than its rivals. The maximum hop count of the CDMA star NoC router is lower than that of the compared topologies due to the concurrent transmission of packets through the router. The CDMA interconnect topology presented in [21] and [22] is made scalable either by doubling the number of chips in the Walsh code set to double the number of ports that can be connected to the router or by using more routers in a star or mesh fashion. The CDMA encoding and decoding operations are local to the router, and therefore, the same Walsh codes can be reused in each NoC router.

A CDMA-based multicast switch has been employed in a 2-D mesh NoC in [23]. The CDMA-based switch allows simultaneous packet transmission due to code-space multiplexing. This approach reduces the hop count in multicasting schemes and allows packets to reach the destination PEs simultaneously, which is preferred in real-time applications. A 14-node CDMA-based network has been developed in [24]. The assignment of spreading codes to TX-RX pairs is dynamic based on the request from each node. Two architectures have been introduced in the CDMA-based network: a serial CDMA network, where each data chip in the spreading code is sent in one clock cycle, and a parallel CDMA network, where all data chips are sent in the same cycle. The CDMA-based serial and parallel networks have been compared with a conventional CDMA network, a mesh-based NoC, and a TDMA bus. For the same network area, the bandwidth of the parallel CDMA network is higher than the throughput of the mesh-based NoC and the TDMA bus due to the simultaneous medium access nature of CDMA.

Standard basis codes are proposed as a replacement to Walsh CDMA codes in [25]. Standard basis codes resemble the TDMA signaling scheme because each code consists of only a single chip of one and the remaining chips are zeros. The orthogonality of TDMA codes is attributed to that the phase shift of the one chip is an integer number of the code duration indicating that the cross correlation between various codes is zero. The orthogonality of TDMA codes enables them to replace the Walsh codes as spreading and despreading CDMA

codes, which reduces the complexity of the channel adder and decoder as the maximum sum of the TDMA codes is one.

Most related works proposing CDMA for on-chip interconnects investigate only architectural and topological enhancements of the basic wireless spread spectrum CDMA scheme. In this paper, a different aspect of the CDMA technology for on-chip interconnects is addressed, which is increasing the interconnect capacity by applying overloaded CDMA to the existing on-chip CDMA-based NoC routers. To the best of our knowledge, we are the first group to investigate this specific point in this paper and its precedings [14], [15].

III. Preliminaries

In this section, overloaded CDMA in wireless communications and the requirements of its on-chip interconnect counterpart and preliminaries of the classical on-chip CDMA switch presented by Nikolic *et al.* [16] are presented.

A. Overloaded CDMA in Wireless Communications

Direct sequence spread spectrum CDMA (DSSS-CDMA) is a leading approach for medium sharing in wireless communications where a set of orthogonal spreading codes composed of a stream of chips of length N are multiplied by the transmitted data bits such that each data bit is spread in N cycles [26, Ch. 2]. A unique spreading code is assigned to every TX-RX pair sharing the communication channel. Data streams of users sharing the channel are spread and simultaneously transmitted to an additive communication channel. Despreading is achieved by applying the correlation operation to the received sum, where each receiver can extract its data by correlating it with the assigned spreading code. Orthogonality between spreading codes guarantees unique identification of every code received in the channel sum by exploiting the associative and distributive properties of the addition operation carried out by the communication channel. In wireless communications, random effects such as noise, fading, and multipath arising in the communication channel affect proper identification of the received sum, which increases the bit error rate (BER) of the received data.

Unfortunately, the number of orthogonal codes in a spreading code set is usually limited to the spreading code length N, which reduces the channel utilization efficiency. Overloaded CDMA has been proposed in the wireless communication literature to increase the number of spreading codes by adding nonorthogonal codes that can be identified on the receiver side [13]. Increasing the channel utilization comes at the expense of relaxing the orthogonality requirements of the spreading codes and increasing MAI, which consequently increases the BER. The proposed overloaded CDMA spreading codes in wireless communications are accompanied with complicated receiver structures making use of multiuser detection instead of the simple correlator or matched filter receiver employed in basic DSSS-CDMA.

In this paper, we apply the overloaded CDMA concepts developed in the wireless communication field to on-chip interconnects to increase the CDMA-based NoC capacity. However, on-chip interconnects are significantly different from wireless communication channels on both the characteristic and requirement levels. In the following, basic features of overloaded CDMA will be enumerated from the on-chip interconnect perspective to sum up the OCI design considerations.

1) Overloaded CDMA is a medium access technique deployed in wireless communications based on DSSS-CDMA.
2) The complexity of wireless overloaded CDMA limits its applicability for on-chip interconnects, which require simple communication schemes to meet the performance requirements.
3) Despite that wireless CDMA is usually adopted in conjunction with other modulation techniques, only baseband binary CDMA is considered for on-chip interconnects, which can be directly implemented in digital platforms such as FPGAs.
4) Because only digital on-chip interconnects are considered, random effects arising in analog communication channels such as noise, fading, and MAI can be efficiently mitigated using error detection and correction techniques [27]. Therefore, such random effects are neglected in this paper.
5) Consequently, due to the last two assumptions, the complexity of the CDMA receivers can be significantly reduced to fit the on-chip interconnect requirements.

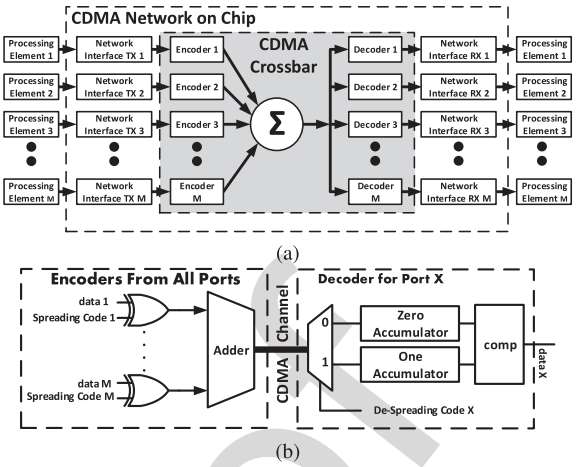

Fig. 1. (a) CDMA NoC router architecture. (b) Classical CDMA crossbar.

B. Classical CDMA Crossbar Switch

Fig. 1(a) illustrates the high-level architecture of a CDMA-based NoC router. The physical layer of the router is based on the classical CDMA switch presented by Nikolic *et al.* [16] and illustrated in Fig. 1(b). The switch is composed of a number of XOR encoders, a channel adder, and accumulator-based decoders. In the encoder, an N-chip length binary orthogonal code, generated from a Walsh spreading code set, is XORed with the transmitted data bit and sent out serially, indicating that a single bit is spread in a duration of N clock cycles. Therefore, the crossbar transaction frequency f_t and operating clock frequency f_c are related as $f_t = f_c/N$. The number of TX-RX ports sharing the CDMA router equals

$M = N - 1$ for Walsh spreading codes. Serial streams from all transmit PEs sharing the crossbar are added together and the binary sum is sent to a decoding circuit feeding the receiving ports. Binary encoding and signaling are preferred over multilevel signaling for implementing the channel adder due to its superior performance, reliability, and its inherent support by digital platforms. The data sent over the CDMA crossbar switch are given by the following equation:

$$S(i) = \sum_{j=1}^{M} d(j) \oplus C_o(j, i) \tag{1}$$

where $S(i)$ is an m-bit binary number representing the channel sum at the ith clock cycle, the crossbar width $m = \lceil \log_2 M \rceil$, $d(j)$ is the data bit from the jth encoder, $C_o(j, i)$ is the ith chip of the jth orthogonal spreading code, and $\oplus$ is the XOR operation. In the ordinary CDMA crossbar, the adder has $M = N - 1$ input bits and $m = \lceil \log_2 M \rceil = log_2 N$ output bits.

The decoder is implemented as a wrapper that cross correlates the serialized channel sum with the signature code assigned to the TX-RX pair. The decoding process is periodic and the decoding cycle lasts for N clock cycles. The despreading operation is realized using a correlator decoder that correlates the received channel sum with the spreading code assigned to the TX-RX pair. As the spreading codes are generated from the bipolar Walsh code family, the correlation process mainly involves two operations: multiplying the received sum by ± 1 according to the spreading code and accumulation. However, multiplication can degrade the router's performance. Fortunately, the spreading codes are bipolar—composed of only (± 1) chips—eliminating the need for the expensive multiplication operation and reducing it to simple addition and subtraction operations.

Two accumulators are used to realize the correlator decoder. According to the assigned CDMA code, the received sum is passed to the zero accumulator when the current chip value is "0" and to the one accumulator when the chip value is "1," which is equivalent to multiplying the crossbar sum by ± 1. At the uth decoder and ith cycle, the inputs to the zero and one accumulators ($\text{In}_z(i)$ and $\text{In}_o(i)$) are given by

$$\text{In}_z(i) = \overline{C_o(u, i)} \cdot S(i), \quad \text{In}_o(i) = C_o(u, i) \cdot S(i) \tag{2}$$

where $C_o(u, i)$ is the despreading chip of the uth decoder.

The one and zero accumulator circuits accumulate their inputs during the decoding cycle and are reset to zero at the end of each decoding cycle. The values held by the zero and one accumulators are given by the following equations:

$$\text{Acc}_z = \sum_{i=1, i \neq j}^{N} \text{In}_z(i), \quad \text{Acc}_o = \sum_{j=1, j \neq i}^{N} \text{In}_o(i) \tag{3}$$

where $0 < i, j \leq N$ and the indexes i and j do not take the same value for both Acc_z and Acc_o.

Consequently, each accumulator adds $N/2$ different inputs during the decoding cycle because the spreading codes are balanced—the number of zeroes equals the number of ones in a balanced code. At the end of the decoding cycle, the decoder has received the sum of spreading codes or their complements encoded according to the data spread by the transmit ports. Decoding the crossbar sum containing an orthogonal code or its complement using other orthogonal codes (cross-correlation) results in adding the same value to both accumulators. Decoding the crossbar sum containing an orthogonal code or its complement using the same code (autocorrelation) makes the value of one accumulator greater than the other accumulator by the number of ones in the code, which equals $N/2$ for balanced spreading codes. The cross correlation between orthogonal codes yields zero, while autocorrelation (multiplying the code by itself or its complement) yields $\pm N/2$. Therefore, the difference between the one and zero accumulators is always $\pm N/2$ for orthogonal spreading codes. This can be directly derived for the accumulator decoder using the correlation definition and Walsh code orthogonal property. For bipolar Walsh codes, the CDMA sum can be written as

$$S = \sum_{j=1}^{M} (-1)^{d(j)} C_o(j) \tag{4}$$

where S is the N-cycle waveform of the crossbar sum, $d(j)$ are the data sent by the jth user, and $C_o(j)$ is the orthogonal code assigned to user j. The decoding operation at the kth receiver is achieved by correlating the crossbar sum by the kth spreading code as follows:

$$R(k) = C_o(k) \cdot S = C_o(k) \cdot \sum_{j=1}^{M} (-1)^{d(j)} C_o(j) \tag{5}$$

$$= \sum_{j=1}^{M} (-1)^{d(j)} C_o(j) \cdot C_o(k) = (-1)^{d(j)} C_o(k) \cdot C_o(k) + \sum_{j=1, j \neq k}^{M} (-1)^{d(j)} C_o(j) \cdot C_o(k) = (-1)^{d(j)} N/2$$

where $R(k)$ is the correlator output of the kth decoder, $M = N - 1$ for orthogonal Walsh codes, the autocorrelation term $C_o(k) \cdot C_o(k)$ yields $N/2$ for a balanced binary spreading code of length N, and the cross-correlation term $C_o(k) \cdot C_o(j)$ yields zero for any orthogonal spreading codes with different $k \neq j$. At the end of the decoding cycle, the difference between the two accumulators is always $N/2$ in the MAI- and noise-free crossbar, e.g., for $N = 8$, the difference between the two accumulators is 4. Comparing the two accumulators directly indicates the encoded data via the sign of $R(k)$; if the zero accumulator's content is greater than the one accumulator's content, the sent data bit is "1"; otherwise, the bit is "0." Therefore, the correlation operation can directly determine the encoded data without errors due to neglecting random effects. The main advantage of the accumulator decoder is replacing the multiplication-based correlator with an addition-based one.

IV. Overloaded CDMA Interconnect

Fig. 1(a) illustrates the high-level architecture of the CDMA-based NoC router. The CDMA router has M transmit/receive ports. The main difference between the overloaded

and classical CDMA routers is that $M > N-1$ for the former due to channel overloading. Each PE is connected to two network interfaces (NIs), transmit and receive NI modules. During packet transmission from a PE, the packet is divided into flits to be stored in the transmit NI first-input first-output (FIFO). The router arbiter then selects M winning flits at most from the top of the NI FIFOs to be transmitted during the current transaction. The selected flits must all have an exclusive destination address to prevent conflicts, and a winner from two conflicting flits is selected according to the router's priority scheme. The employed priority scheme is the fixed winner that takes all priority schemes; only one of the transmitters is given a spreading code and is acknowledged to start encoding. Once done, the router assigns CDMA codes to each transmit and receive NI. NIs with empty FIFOs or conflicting destinations are assigned all-zero CDMA codes such that they do not contribute MAI to the CDMA channel sum. Afterward, flits from each NI are spread by the CDMA codes in the encoder module.

The data are spread into N chips, where N is the CDMA code length that equals the number of clock cycles in a single crossbar transaction. Spread data chips from all encoders are summed by the CDMA crossbar adder and the sum is sent out serially to all decoders. The encoding/decoding process lasts for N clock cycles synchronized via a counter. At each decoder, the assigned code is cross correlated with the received sum to decode the data from the summed chips. The decoded flits are stored in the receive NI FIFOs until they are read by the PEs. In this paper, we focus on the high-level architecture and implementation details of the overloaded CDMA crossbar represented by the gray block in Fig. 1(a).

A store and forward flow control and a deterministic routing algorithm are employed in the OCI router. The routing algorithm lies at the network layer, which is a higher layer than the physical layer containing the crossbar switch. According to the OSI model design principles, each layer of the model exists as an independent layer. Theoretically, one can substitute one protocol for another at any given layer without affecting the operation of layers above or below. Thus, using the same flow control protocol and routing algorithm enables comparing the OCI-based router with SDMA- and TDMA-based routers.

A. OCI Crossbar High-Level Architecture

The main objective of this paper is increasing the number of ports sharing the ordinary CDMA crossbar presented in [17], while keeping the system complexity unchanged using simple encoding circuitry and relying on the accumulator decoder with minimal changes. To achieve this goal, some modifications to the classical CDMA crossbar are advanced. Fig. 2 depicts the high-level architecture of the OCI crossbar for a single-bit interconnection. The same architecture is replicated for a multibit CDMA router. M TX-RX ports share the CDMA router, where spread data from the transmit ports are added using an arithmetic binary adder having M binary inputs and an m-bit output, where $m = \lceil \log_2 M \rceil$. The adder is implemented in both the reference and pipelined architectures. A controller block is used for code assignment and arbitration tasks. Each PE is interfaced to an encoder/decoder wrapper enabling data spreading/despreading.

Unlike orthogonal spreading codes, which are XORed with the binary data bit, an AND gate is utilized to spread data using nonorthogonal spreading codes. The AND gate encoder works as follows: if the transmitted data bit is "0," it sends a stream of zeros during the whole spreading cycle, which does not cause MAI on the channel; if the transmitted data bit is "1," the encoder sends a nonorthogonal spreading code. Therefore, the additional MAI spreading code will either contribute an MAI value of one or zero each clock cycle because the encoder is an AND gate. The XOR encoder of the ordinary CDMA crossbar cannot be used to encode the OCI codes because it only complements the spreading code chips, so an XOR gate will cause MAI to the crossbar whether the data bit is "0" or "1." A hybrid encoder is developed for both orthogonal and nonorthogonal spreading with an XOR gate, an AND gate, and a multiplexer unit, as shown in Fig. 2. Two decoder types are implemented for orthogonal and nonorthogonal data. More details about each component of the OCI crossbar will be presented in Section IV-C after describing the OCI code design procedures and decoding scheme in Section IV-B.

B. OCI Code Design

The Walsh–Hadamard spreading code family has a featured property that enables CDMA interconnect overloading. The difference between any consecutive channel sums of data spread by the orthogonal spreading codes for an odd number of TX-RX pairs M is always even, regardless of the spread data. This property means that for the $N-1$ TX-RX pairs using the Walsh orthogonal codes, one can encode additional $N-1$ data bits in consecutive differences between the N chips composing the orthogonal code. Thus, exploiting this property enables adding 100% nonorthogonal spreading codes, which can double the capacity of the ordinary CDMA crossbar. In this section, the code design methodology, mathematical foundations, and the decoding details of both T-OCI and P-OCI codes are provided. The notations used throughout this paper are listed in Table I.

An AND gate encoder is used to encode data with nonorthogonal spreading codes as shown in Fig. 2(a). Therefore, for a nonorthogonal encoder, if data to transmit are one, a single spreading chip at a specific time slot in the spreading cycle is added to the channel sum, which causes the consecutive sum difference to deviate. The nonorthogonal codes imitate the TDMA signaling scheme as each code is composed of a single chip of "1" sent in a specific time slot. The encoding/decoding scheme presented in this paper provide a novel approach that enables coexistence between CDMA and TDMA signals in the same shared medium. Therefore, the developed encoder is called TDMA overloaded on CDMA interconnect (T-OCI). Fig. 3 shows an encoding/decoding example of two T-OCI codes for a spreading code of length $N = 8$. An odd number of orthogonal codes must be used simultaneously to preserve the even difference property of Walsh codes.

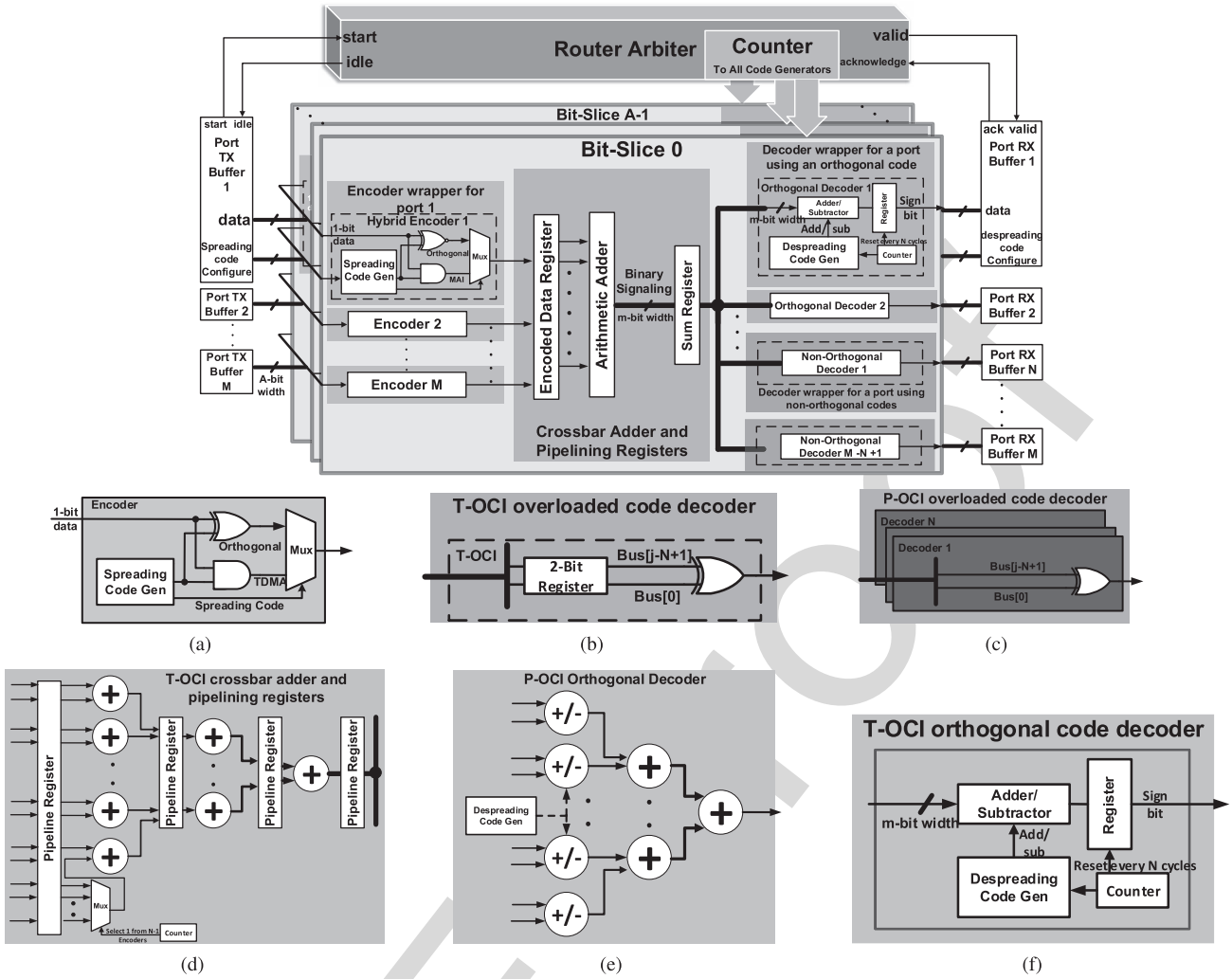

Fig. 2. High-level architecture and building blocks of the OCI crossbar. (a) T-OCI/P-OCI hybrid encoder. (b) T-OCI nonorthogonal decoder. (c) P-OCI nonorthogonal decoder. (d) T-OCI pipelined crossbar tree adder, in which the adder is replicated N times for P-OCI crossbar. (e) P-OCI orthogonal decoder. (f) T-OCI orthogonal decoder.

TABLE I
DEFINITION OF NOTATIONS

Notation	Description
N	Orthogonal spreading code Length
M	Number interconnected ports
m	Number of crossbar adder wires
S	Sum of CDMA chips carried by the channel
d_C	Data bit encoded by an orthogonal CDMA code
d_T	Data bit encoded by a non-orthogonal TDMA code
$C_o(j)$	The j^{th} chip of the orthogonal CDMA code
$T(j)$	The j^{th} chip of the non-orthogonal TDMA code
C_n	TDMA MAI code (non-orthogonal spread data)
$R(k)$	Output of the k^{th} correlator decoder

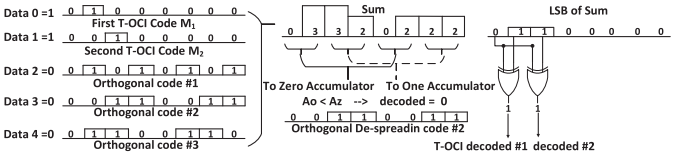

Fig. 3. Encoding/decoding of three orthogonal codes and two T-OCI codes.

TDMA codes cause MAI to the sum of CDMA spread data. The equation of the crossbar sum for both CDMA and TDMA encoded data can be written as

$$S = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + \sum_{j=N+1}^{2N-1} d_T(j) \cdot T(j-N+1) \quad (6)$$

where S is the N-cycle waveform of the channel sum, $d_C(j)$ is the orthogonal CDMA data bit sent by the jth user, $d_T(j)$ is the nonorthogonal TDMA data bit sent by the jth, $C_o(j)$ is the orthogonal code assigned to the jth user, and $T(j-N+1)$ is the TDMA code assigned to the jth user. The TDMA code $T(i)$ is a single chip of "1" assigned at the ith time slot. The TDMA term of the equation is the sum of products of TDMA chips and their corresponding data bits. This term can be viewed as another N-chip spreading code added to the orthogonal spread data represented by the first term of the equation. It should be indicated that the first chip of the TDMA MAI code is always set to zero ($T(1) = 0$), and the remaining $N-1$ chips are assigned according to the encoded data bits;

this note is the key to properly decode both orthogonal and nonorthogonal spread data. Equation (6) can be rewritten as follows:

$$S = \sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T) \tag{7}$$

where $C_n(d_T)$ is the TDMA MAI code as a function of the nonorthogonal data. The number of the crossbar adder output bits is $m = \log_2 N + 1$ despite that the number of adder inputs is $2(N-1)$, which is the total number of orthogonal and nonorthogonal TX-RX pairs sharing the OCI crossbar. This is because at any time instance, there can be only N inputs having a value of "1" in the T-OCI encoding scheme. The number of the adder output bits is specifically important because it directly determines the crossbar wiring density.

Orthogonal spread data can be still decoded properly using the accumulator-based correlator. Despreading of the kth orthogonal spread data is achieved by multiplying the crossbar sum by the kth orthogonal spreading code as follows:

$$\begin{aligned} R(k) &= C_o(k) \cdot S = C_o(k) \left(\sum_{j=1}^{N-1} (-1)^{d_C(j)} C_o(j) + C_n(d_T) \right) \\ &= (-1)^{d_C(j)} N/2 + C_o(k) \cdot C_n(d_T). \end{aligned} \tag{8}$$

The first term of (8) is the autocorrelation term, which is equal to $\pm N/2$ according to the data spread d_C, while the second term is the cross correlation between the orthogonal spreading code $C_o(k)$ and the nonorthogonal MAI TDMA code $C_n(d_T)$. The maximum MAI value contributed by the second term is $\pm N/2$ because the MAI code is correlated with a balanced orthogonal code, where the number of "1" chips is equal to the number of "0" chips and equals $N/2$. This case can only occur if the MAI TDMA code constructed by the nonorthogonal encoded data is identical to $C_o(k)$ or its complement $\overline{C_o(k)}$, which yields $\pm N/2$, respectively.

As long as the MAI magnitude $|C_o(k).C_n(d_T)| < N/2$, the nonzero correlation result will always facilitate proper decoding of the orthogonal data, where the comparator circuit can still be used to detect the accumulator sign. The main challenge is decoding orthogonal data when the MAI TDMA code is identical to the spreading code or its complement, which might cause the correlation result to be zero. Zero correlation indicates either cases of [$d_C = 0$ and $C_n(d_T) = \overline{C_o(k)}$] or [$d_C = 1$ and $C_n(d_T) = C_o(k)$]. However, because the first chip of the MAI TDMA code $C_n(d_T)$ is always forced to zero, the first case can be excluded because all Walsh orthogonal spreading codes start with "0." Therefore, the zero correlation result always indicates that the orthogonal data encoded is "1."

On the other hand, decoding nonorthogonal TDMA data can be achieved by exploiting the even difference property of the Walsh orthogonal codes. Because the T-OCI decoding is achieved by parity checking the difference between consecutive crossbar sums, a two-input XOR gate is used. The XOR gate inputs are the current least significant bit (LSB) of the crossbar sum and the LSB of the crossbar sum corresponding to the first chip of the Walsh codes stored in a flip-flop (FF)

$$d_T(j) = S(0) \oplus S(j - N + 1). \tag{9}$$

The XOR gate output determines the parity of the difference, and consequently, the nonorthogonal TDMA encoded data.

The P-OCI crossbar employs the same Walsh and Overloaded Codes as the T-OCI crossbar; however, the data spreading and decoding are parallelized. Instead of using one XOR gate to encode the data bit using the spreading code, N XOR gates are used where the data bit is XORed with the N chips of the spreading code in parallel. The nonorthogonal AND gate encoders are also replicated N times. Since the N chips are available in parallel in the same clock cycle, N replicas of the crossbar adder are necessary to add the N chips from each transmit port. Therefore, the encoding and decoding equations governing P-OCI are the same as those of the T-OCI.

C. OCI Crossbar Building Blocks

Two variants are realized for each OCI crossbar, reference and pipelined architectures. The pipelined architecture is implemented to increase the crossbar operating frequency, and consequently, bandwidth by adding nonfunctional pipelining registers to reduce the crossbar critical path. The OCI crossbar shown in Fig. 2 is basically composed of three main building blocks: 1) the encoder wrappers; 2) the decoder wrappers; and 3) the crossbar adder blocks, which are described in the following.

1) *Crossbar Controller:* At the beginning of each crossbar transaction, the controller assigns spreading codes to different encoders. The assignment of orthogonal despreading codes to receive ports is fixed, i.e., does not change between the crossbar transactions. Therefore, for a router port to initiate the communication with the receive port it addresses, its encoder must be assigned a spreading code that matches the destined decoder. If two different ports request to address the same decoder, the controller allows one access and suspends the other according to a predefined arbitration scheme. This code assignment scheme is called receiver-based protocol [20]. In this paper, a static allocation scheme that allocates fixed spreading codes to all encoders is used. To interconnect a large number of PEs, a torus, star, or hybrid NoC topology can be realized where the assignment of spreading codes is local to each router. Consequently, each new packet arriving at a router is assigned a spreading code corresponding to its exit port decoder. The crossbar controller issues handshake signals to the transmit and receive ports with matching spreading codes to enable the transmitter encoders and receiver decoders.
2) *Hybrid Encoder:* The encoder is hybrid, it can encode both orthogonal and nonorthogonal data. A transmitted data bit is XORed/ANDed with the spreading code to produce the orthogonal/nonorthogonal spread data, respectively. A multiplexer chooses between the orthogonal and nonorthogonal inputs according to the code type assigned to the encoder as depicted by Fig. 2(a). The encoder is replicated N times for the P-OCI crossbar.

TABLE II

COMPLEXITY ANALYSIS OF THE CONVENTIONAL CDMA AND OCI CROSSBARS FOR N-CHIP SPREADING CODES (FOR A GENERIC NUMBER OF PORTS $2(N-1)$); BOLD NUMBERS BETWEEN BRACKETS ARE NUMERICAL VALUES COMPUTED FOR $N = 8$ AS AN ILLUSTRATIVE EXAMPLE

Topology	Instances	Crossbar Wires	Encoders	Orthogonal Decoders		Non-orthogonal decoders		Counters
		FF	COMB	FF	COMB	FF	COMB	
Conventional CDMA Crossbar	Encoders: $N-1$ **(7)**, Orthogonal decoders: $N-1$ **(7)**	$\lceil log_2(N) \rceil$ **(3)**	1-AND	$\lceil log_2((N/4)*(N-1)) \rceil$ **(4)**	Adder output width: $(\lceil log_2((N/4)*(N-1)) \rceil)$ **(4)**	0	0	Adder wires: $\lceil log_2(N) \rceil$ **(3)**
T-OCI Crossbar	Encoders: $2(N-1)$ **(14)**, Orthogonal decoders: $N-1$ **(7)**, T-OCI Decoders: $N-1$ **(7)**	$\lceil log_2(N+1) \rceil$ **(4)**	1-AND, 1-XOR, 1-MUX	$\lceil log_2((N/4)*(N-1)) \rceil + 1$ **(5)**	Adder output width: $(\lceil log_2((N/4)*(N-1)) \rceil + 1)$-bit **(5)**	2	1-XOR	FFs: $\lceil log_2(N) \rceil$ **(3)**
P-OCI Crossbar	Encoders: $2N(N-1)$ **(112)**, Orthogonal decoders: $N-1$ **(7)**, T-OCI Decoders: $N-1$ **(7)**	$N\lceil log_2(N+1) \rceil$ **(4)**	N-AND, N-XOR, N-MUX	0	Adders: $\sum_{i=0}^{log_2 N-1} (log_2 N - i)$ **(6)**	0	1-XOR	

3) *Crossbar Adder:* For a spreading code set of length N, the number of crossbar TX-RX ports is equal to $M = 2(N-1)$. In the T-OCI crossbar, sending a "1" chip to the adder is mutually exclusive between nonorthogonal transmit ports according to the T-OCI encoding scheme. This indicates that among the $2(N-1)$ inputs to the adder, there are guaranteed $(N-2)$ zeros, while the maximum number of "1" chips is N. Therefore, a multiplexer is instantiated to select only a single input of the nonorthogonal TDMA encoded data bits and discard the remaining bits that are guaranteed to be "0." Thus, the adder has only N-bit inputs, $N-1$ from orthogonal encoders, and 1 from the multiplexer, as shown in Fig. 2(d). The sum produced by the adder circuit needs ($\log_2 N$) wires. The number of needed stages of registers to pipeline the adder is ($\log_2 N$), as depicted in Fig. 2(d). N replicas of the crossbar adder are instantiated for the parallel encoding adopted in the P-OCI crossbar.
4) *Custom Decoder:* There are four decoder types for different CDMA decoding techniques: the orthogonal T-OCI and P-OCI decoders and the overloaded T-OCI and P-OCI decoders. The orthogonal T-OCI decoder is an accumulator implementation of the correlator receiver. $N-1$ accumulator decoders are instantiated in all CDMA crossbar types for orthogonal data despreading. Instead of implementing two different accumulators (the zero and one accumulator), an up–down accumulator is implemented and the accumulated result is the difference between the two accumulators of the conventional CDMA decoder as shown in Fig. 2(f). The accumulator adds or subtracts the crossbar sum values according to the despreading code chip and resets every N cycles. The sign bit of the accumulated value directly indicates the decoded data bit, where the positive sign is decoded as "1," while the negative sign is decoded as "0." The P-OCI orthogonal decoder shown in Fig. 2(e) differs from the T-OCI orthogonal decoder in receiving the adder sum values concurrently not sequentially; therefore, the accumulator loop is unrolled into a parallel adder.

The T-OCI overloaded decoder depicted in Fig. 2(b) is composed of a 2-bit register to store the LSBs of two sum values, first of which is $S(0)$ and the second is $S(j-N+1)$, where j is the number of the T-OCI decoders ($N \leq j \leq 2N-2$). The two bits are fed to the XOR gate, which decodes nonorthogonal spread data. The T-OCI decoder is replicated N times to implement the P-OCI decoder of Fig. 2(c). The 2-bit register is not needed anymore because the $S(0)$ and $S(j-N+1)$ values exist in the same cycle. The T-OCI and P-OCI crossbar architectures contain $(N-1)$ orthogonal decoders and $(N-1)$ overloaded decoders.

Table II provides a comprehensive complexity analysis of the OCI crossbars compared with that of the classical CDMA crossbar as a function of the spreading code length N. The complexity of all crossbar components is analyzed and expressed in terms of the number of FFs and combinational logic (COMB). Some crossbar components like the counter can be replicated M times, one replica is used in each decoder. However, the number of such replicated components can be reduced if different decoders can share one replica. Therefore, there is a tradeoff between resource sharing, which reduces resource utilization but increases the wiring density and resource replication. For the orthogonal CDMA decoder, the maximum number of ones the accumulator can add at any decoding cycle is $(N-1)$ ones ("1" from each encoder). The accumulator adds the received crossbar sum up for $N/2$ cycles and subtracts it for $N/2$ cycles, due to the balanced nature of the Walsh orthogonal codes. During any $N/2$ cycles, there only exists $N/4$ "1" chips in each of the $N-1$ codes due to the orthogonality property. Therefore, the value stored in the accumulator never exceeds $N(N-1)/4$ for orthogonal codes only. Thus, the accumulator and its pipelining register are $\lceil log_2(N(N-1)/4) \rceil$ wide. For the OCI decoder, an additional bit is added to the accumulator output due to increasing the maximum sum value by 1.

For the same number of chips N, the conventional CDMA and T-OCI crossbar variants exhibit the same latency, which is N clock cycles because a single data bit is spread in N chips. The latency of the P-OCI crossbar, however, is only one cycle. The conventional CDMA crossbar utilizes the least area, while the P-OCI crossbar utilizes the largest area due to the additional $N-1$ hybrid encoders and $N-1$ XOR decoders per spreading chip. However, the area normalized to the number of ports in the T-OCI crossbar is lower than

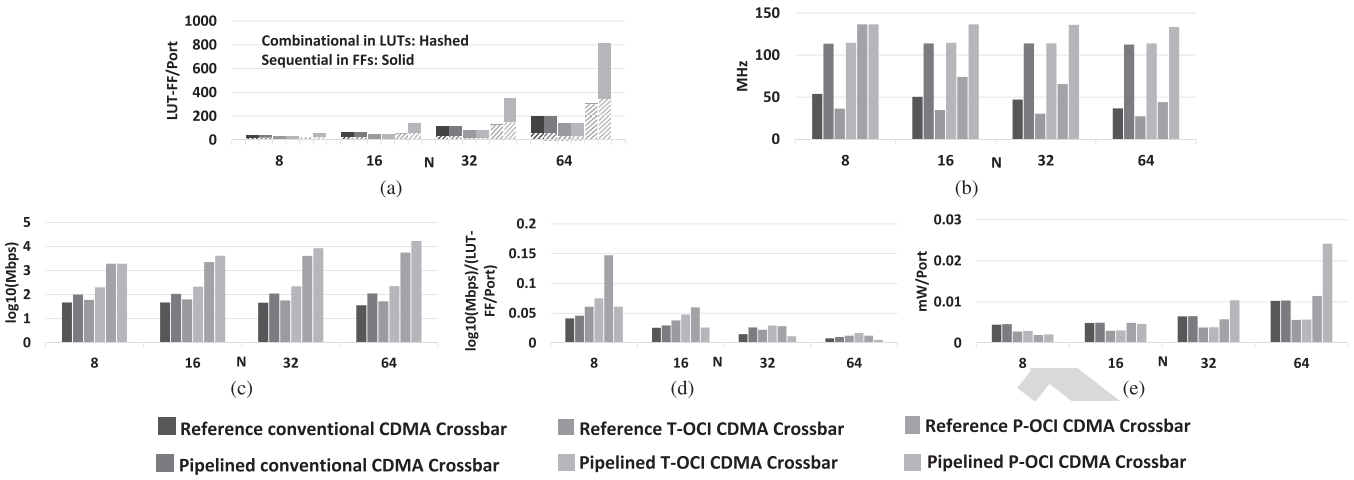

Fig. 4. Implementation results of the OCI crossbars for a spreading code length $N = \{8, 16, 32, 64\}$. (a) Resources as combinational (hashed bars) and noncombinational (solid bars) in LUT-FF/port. (b) Maximum clock frequency f_c in megahertz. (c) Log-scaled crossbar bandwidth BW in megabits per second. (d) Dynamic power dissipated P_D in milliwatts per port. (e) Dynamic power dissipated P_D in mw/port

that in the conventional CDMA crossbar. The P-OCI crossbar bandwidth, however, is the highest of the three crossbars. The T-OCI crossbar bandwidth is double that of the conventional CDMA crossbar because the number of interconnected ports is doubled, while the P-OCI bandwidth is $N \times 100\%$ higher than that of the T-OCI crossbar. Therefore, the P-OCI crossbar has the highest bandwidth at the expense of higher complexity, while the conventional CDMA crossbar has the lowest bandwidth and complexity and the T-OCI crossbar seizes the middle ground in terms of area and bandwidth.

V. Performance Evaluation

In this section, the performance evaluation results of the developed OCI crossbars are presented.

A. OCI Crossbar Evaluation

In this section, a comparison among the conventional CDMA, T-OCI, and the P-OCI crossbars is drawn. A crossbar containing a number of TX-RX ports is built with full capacity, i.e., the number of ports is the maximum number offered by the crossbar. All CDMA crossbar architectures in both the reference and pipelined variants are implemented and validated on an Artix-7 AC701 evaluation kit. The developed crossbars are evaluated for different spreading code lengths $N = \{8, 16, 32, 64\}$. To establish a fair comparison among different crossbar architectures with different numbers of ports, all utilization metrics are normalized to the number of crossbar ports M. The evaluation results, including the resource utilization expressed in the number of lookup tables (LUTs) and FFs per port, maximum crossbar frequency, dynamic power consumption per port, and crossbar bandwidth, are illustrated in Fig. 4.

As depicted in Fig. 4(a), for a spreading code of length N, the resource utilization per port of the T-OCI crossbar is lower than that of the ordinary CDMA crossbar by 31%. This salient reduction in the normalized resource utilization is due to the significant increase in the CDMA interconnect capacity compared with the marginal overhead added by the crossbar circuitry. On the other hand, the P-OCI crossbar is 400% larger than the conventional CDMA crossbar due to the parallel crossbar adders. Increasing the spreading code length N increases the resource utilization per port, due to the increasing crossbar complexity. Specifically, with increasing N, the size of the crossbar adder and accumulator decoder circuitry increases. The resource utilization of all crossbar pipelined variants is always larger than that of the basic architectures due to the additional nonarchitectural pipelining registers.

For all reference architectures, the operating frequency is limited by the critical path length of the crossbar adder. For various CDMA crossbars of the same spreading code length N, orthogonal spreading and despreading circuits are identical and nonorthogonal data encoders and decoders are running parallel to the orthogonal spreading circuitry with a shorter critical path length. The input size of the adder circuit is equal to M, the number of transmitting ports, which varies with the CDMA crossbar type. Fig. 4(b) illustrates that for a spreading code of fixed length N, the crossbar frequency of the overloaded CDMA crossbars is lower than the basic CDMA crossbar frequency due to the increase in the adder circuit size. The pipelined architecture splits the adders' critical path into $\lceil \log_2(N+1) \rceil$ stages, which improves the maximum crossbar frequency at the expense of the extra nonarchitectural registers and output latency. The maximum crossbar frequency in the pipelined architectures no longer depends on the adder, yet it depends on the maximum delay of both the adder stage and I/O circuitry. The crossbar frequency decreases with increasing N for both overloaded and ordinary CDMA crossbars due to the increasing computational complexity of the adders, as shown in Fig. 4(b). The clock frequency of the P-OCI crossbar is higher than that of the T-OCI crossbar due to the absence of the highly loaded synchronization counters and some pipelining registers presented in the T-OCI crossbar.

With increasing N, the drop in the maximum clock frequency is compensated for by the increase in the

crossbar bandwidth, due to the capacity enhancement gained by crossbar overloading as shown in Fig. 4(c). The log-scaled crossbar bandwidth is plotted for only a single bit per port interconnected via the CDMA crossbar. For a fixed N, the enhancement of the CDMA crossbar bandwidth for the P-OCI and T-OCI crossbars over the classical CDMA crossbars is salient. Generally, the CDMA crossbar bandwidth BW is given by the following equation:

$$BW = W \ f_c \ \frac{M}{\Gamma} \tag{10}$$

where W is the port width in bits, f_c is the crossbar clock frequency, M is the number of crossbar ports, and Γ is the number of cycles to encode 1 bit of data from all ports. The T-OCI crossbar bandwidth demonstrates a significant increase over the ordinary CDMA crossbar as it has an overloading ratio of $M/N = 2$ compared with the basic CDMA crossbar ratio of $M/N = 1$ for the same $\Gamma = N$ for both crossbars. For the P-OCI crossbar, however, $\Gamma = 1$, and therefore, the bandwidth of the P-OCI crossbar is N times that of the T-OCI crossbar and $2N$ times that of the conventional CDMA crossbar. Fig. 4(d) depicts the bandwidth-to-resource ratio; the T-OCI and P-OCI crossbars offer higher ratios compared with the conventional CDMA crossbar due to the significant bandwidth enhancement compared with the induced marginal resource overhead.

As illustrated in Fig. 4(e), for a spreading code of fixed length N, the dynamic power dissipation per port, estimated by the Xilinx Vivado tool for a single crossbar transaction, is decreased by 45% for the T-OCI crossbar due to the offered capacity enhancement. However, due to the increased area and parallel encoding–decoding of the P-OCI crossbar, its dynamic power dissipation is 133% higher than that of the conventional CDMA crossbar. With increasing N, power dissipation per port increases for all CDMA crossbars due to the increased size and complexity of the crossbar components.

B. OCI Communication Reliability Considerations

Since the OCI scheme relies on adding detectable interference to the interconnect, the robustness of the OCI crossbar to noise may be raised as a concern; would the added MAI reduce the robustness of the OCI compared with that of the conventional CDMA interconnect? According to [27], while full-swing digital implementations have typically been able to assume BER values less than 10^{-15} over the operating range of voltages and frequencies, this assumption does not hold true for custom low-swing interconnect implementations and modern deep submicrometer circuits. Indeed, in wireless communication channels, overloaded CDMA would increase the BER compared with the classical CDMA because of overloading the channel with MAI. Wireless channels are purely analog exposing them to all random effects such as noise. On the other hand, the OCI crossbar adopts binary signaling to carry the crossbar sum instead of multilevel or analog signaling. The binary nature of the OCI interconnect enables enhancing its robustness by employing error detection and correction techniques to mitigate such random effects.

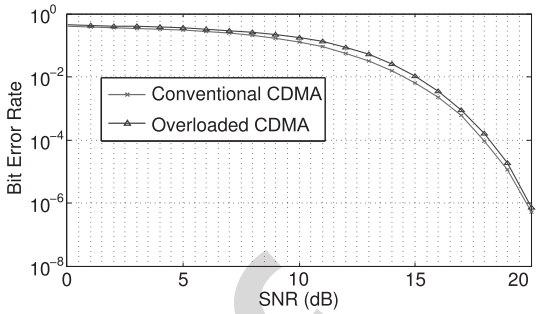

Fig. 5. BER versus SNR of the OCI and conventional CDMA crossbars in the presence of AWGN.

To empirically test the robustness of the OCI crossbar on the FPGA platforms, a testbench was applied for $N = 16$ OCI crossbar implemented on a Zedboard FPGA evaluation kit with a 100-MHz clock frequency and a 1 V core voltage. Zynq's embedded processor runs a program generating 10^6 consecutive crossbar transactions and compares the decoded output with the input data. Zero errors were detected during the experiment, which lasted for 27 h.

On the other hand, to study the reliability of OCI and conventional CDMA links in the presence of error sources such as noise, the BER of the overloaded and classical CDMA links subject to additive white Gaussian noise (AWGN) with a variable signal-to-noise ratio (SNR) was computed using MATLAB simulation for the following test scenario: the CDMA sum S can be expressed as a bit vector $S = [s_1 \ s_2 \ \ldots \ s_m]$, where $m = \lceil \log_2 M \rceil$. An AWGN vector of size m is added to the sum S to generate the corrupted sum $\tilde{S}$ such that $\tilde{S} = S + [N_1 \ N_2 \ \ldots \ N_m]$, where each N_i is an AWGN with zero mean and variance $\sigma^2 = \text{Ps/SNR}$, where Ps is the signal power. A total of 10^7 test vectors are randomly generated per SNR value, which changes from 0 to 20. The BER–SNR curves shown in Fig. 5 depicts an increase in the BER of overloaded CDMA compared with that of classical CDMA in a digital communication channel subject to AWGN. The BER increase is no greater than 72% and its average is 35%.

C. OCI for NoCs: Analytical Evaluation

Table III provides an analytical comparison between the OCI crossbars and some existing bus and NoC interconnection techniques. The comparison is established for an interconnect of M TX-RX pairs representing the number of ports in an NoC router. The compared metrics are the interconnect complexity normalized to the port width in bits W, interconnect latency in clock cycles, and the interconnect bandwidth normalized to the crossbar operating frequency f_c and W.

As a bus, the OCI crossbar provides a higher bandwidth than the CDMA peripheral bus [16]. The CDMA peripheral bus interfaces multiple peripherals to multiple PEs on a shared CDMA bus. The OCI technique can be applied to the peripheral bus to increase the number of interconnected PEs and peripherals without degrading the transaction latency. In the CDMA parallel transfer wrapper of [17] and [18],

TABLE III
ANALYTICAL COMPARISON BETWEEN THE T-/P-OCI CROSSBARS AND OTHER INTERCONNECTS

Bus/NoC Topology	Complexity / W	One packet Latency (clock cycles)	$BW/(f_c \times W)$
T-OCI Crossbar	M Hybrid encoders $M/2$ Accumulator decoders $M/2$ XOR decoders	$M/2$	2
P-OCI Crossbar	M^2 Hybrid encoders $M/2$ Accumulator decoders $M/2$ XOR decoders $M/2$ adders	1	$2M$
TDMA-based CDMA NoC [25]	M AND Encoders M Accumulator decoders	M	1
CDMA Peripheral bus [16]	M Encoders M Accumulator decoders	M	1
CDMA Parallel Transfer Wrapper [17], [18]	M Encoders M Accumulator decoders	M	1
CDMA NoC [20]	M Encoders/router M Accumulator decoders	1 hop M per hop	1
PTP NoC [20]	One Bypass multiplexers/router	1 hop (best case) M hops (worst case)	M (best case) $1/M$ (worst case)
CDMA star NoC [22]	M Encoders/router M Accumulator decoders	1 hop (best case) 3 hops (worst case)	*N.A.*
Mesh NoC with CDMA Multicastable Router [23]	M Encoders/router M Accumulator decoders	5 hops worst case in 5×5 mesh	*N.A.*
Mesh NoC without CDMA Multicastable Router [23]	*N.A.*	8 hops worst case in 5×5 mesh	*N.A.*
Parallel Dynamic CDMA NoC [24]	M^2 Encoders/router M Accumulator decoders	1 hop 1 per hop	M
Mesh NoC [28]	M buffers/router $M \times M$ SDMA cross bar/router	1 hop 1	M
MPEG-2 PTP [29]	M ports (wiring)	1	M
MPEG-2 NoC [29]	M buffers/router $M \times M$ SDMA cross bar/router	1 hop 1 per hop	M
MPEG-2 TDMA Bus [29]	M ports (wiring) arbiter	1	1

the number of parallel transfer lines is reduced by bundling data using spreading codes. The OCI spreading codes can be used to bundle more data bits on the same number of wires. Therefore, the OCI crossbar can provide higher bandwidth than the CDMA peripheral bus and the CDMA parallel transfer wrapper of the same complexity due to crossbar overloading.

The CDMA encoding–decoding scheme presented in [25] is based on the standard basis TDMA codes, which replace the orthogonal Walsh codes. The encoders are consequently replaced by an AND gate, the bus adder is reduced to a single XOR gate, the channel wires are reduced to one wire per bit because no two TDMA chips are simultaneously sent in the same clock cycle. This scheme resembles TDMA signaling but adopts the CDMA arbitration procedures where the code assignment is done once every N encoding–decoding bus cycle. On the other hand, our proposed OCI technique enables coexistence between both CDMA and TDMA codes on a single channel, providing double bandwidth, while utilizing less area than two independent TDMA and CDMA crossbars.

The data transfer latency of the CDMA NoC router in [20] is equal to the best case latency of a PTP network. This data transfer latency of the CDMA router can be reduced using fewer chips per spreading code while keeping the number of PEs unchanged through utilizing the OCI technique. The CDMA NoC router in [22] utilizes the orthogonal Walsh code set to interconnect a maximum of N network nodes, where N is the number of chips in a spreading code. The presented

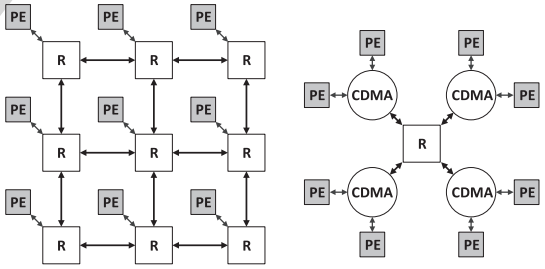

Fig. 6. (a) CONNECT torus topology (b) versus the OCI star topology.

routers can exploit the OCI schemes to double the number of ports of the network router without increasing the spreading code length and hence without increasing the hop latency. The multicast router of [23] interconnects four ports and four PEs. The OCI technique can double the capacity of the switch without increasing the hop latency, and therefore, each PE can multicast more packets through the router in one hop.

The modules of the MPEG-2 encoder in [29] are interconnected using PTP, NoC, and TDMA bus topologies to evaluate these three different interconnects. The NoC is shown to have a close bandwidth to a PTP at fewer logic resources and wiring area and much higher bandwidth than the TDMA bus. The conventional parallel CDMA buses of [24] demonstrate equal bandwidth to the best case bandwidth of mesh NoCs [28], in addition to the fixed latency, due to the simultaneous medium access by the interconnected PEs. The P-OCI crossbar can

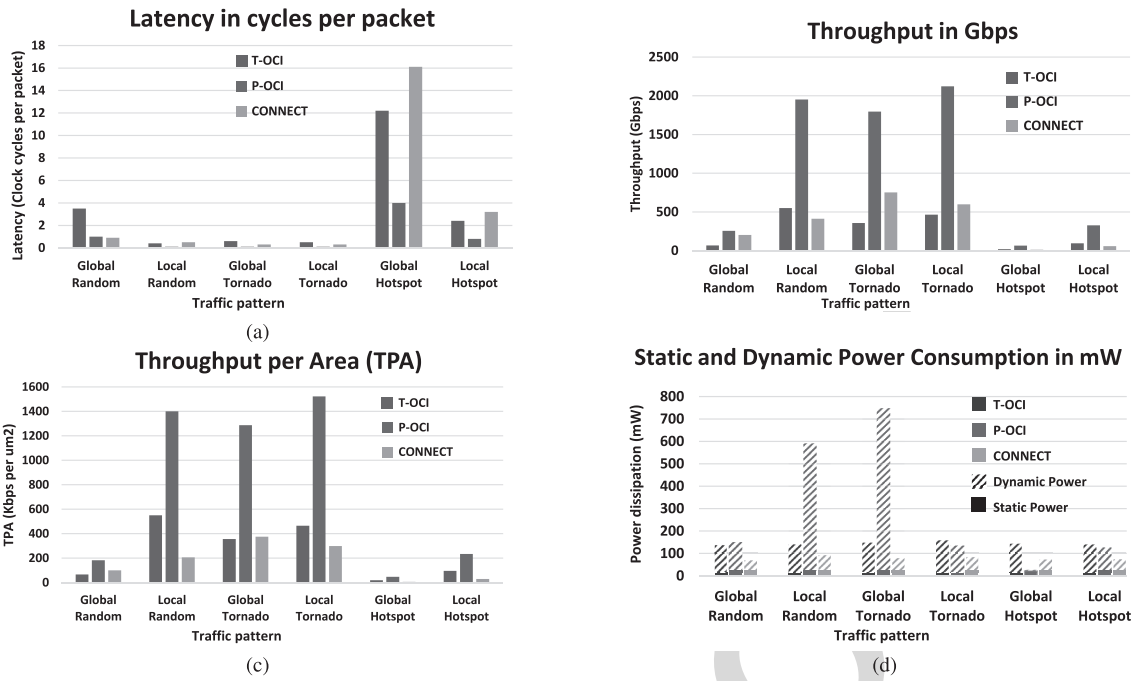

Fig. 7. (a) Latency, (b) throughput, (c) TPA, and (d) power dissipation of T-OCI, P-OCI, and CONNECT NoCs.

provide a higher bandwidth and a lower latency than the conventional parallel CDMA buses by simultaneously transmitting all the N chips of the spreading code in parallel due to overloading. This analytical discussion highlights the OCI capability of substituting the classical CDMA interconnect in any CDMA-based bus or NoC architecture while providing higher bandwidth at the same latency or interconnecting the same number of ports at lower latency per transaction.

D. OCI for NoCs: Experimental Evaluation

To study the effectiveness of the OCI crossbar in a full working NoC, a 65-node star topology is built using five OCI routers, each of the 13 PEs is connected by an OCI router with $N = 8$, and the five OCI routers are interconnected by an SDMA central router. Both T-OCI- and P-OCI-based NoCs are compared with a 64-node, 16-bit flit, and 8-ary 2-cube torus SDMA-based NoC generated by the CONNECT tool [30]. The CONNECT NoC employs simple input queued routers with peek flow control. Fig. 6 illustrates the torus topology employed by the CONNECT NoC versus the star topology adopted by the OCI NoC. The star topology is chosen for the OCI NoC since the improvement of the OCI complexity against the SDMA router increases as the number of ports increases due to the linear increase in the OCI crossbar area compared to the quadratic increase in the SDMA crossbar area. Similarly, the torus topology was chosen for the CONNECT NoC since the torus SDMA crossbars have a low number of ports, which is translated to lower complexity. Since each router in a torus network accommodates five buffers, the buffer spacing offered in the CONNECT NoC is 64×5, while the spacing of the OCI-based NoC is equal to the number of PEs plus the number of buffers in the central router, which equates to $65 + 5$. Therefore, to equalize the buffer spacing in the compared NoCs, the OCI buffer width is sized four times the CONNECT buffer width. Consequently, the flit size of the OCI-based NoC is 64 bits. Table IV lists the implementation results of the three NoCs on the 65-nm ASIC technology, the area of the T-OCI NoC is 45% less than that of the CONNECT NoC, while the area of the P-OCI is 30% less than that of the CONNECT NoC, despite the larger flit size with a reduction in latency due to their lower complexity.

TABLE IV
IMPLEMENTATION RESULTS ON THE ASIC 65-*nm* TECHNOLOGY

	CONNECT	T-OCI	P-OCI
Area (mm^2)	1.998	1.09	1.394
Clock period (ns)	0.72	1.11	1.36

The performance comparisons of the T-OCI and P-OCI NoCs versus the CONNECT NoC are depicted in Fig. 7 for six synthetic traffic patterns and for the same packet width of 256 bits. The uniform, hotspot, and tornado traffic patterns are employed with two variants: local and global traffic. In the global traffic, the traffic pattern is applied to the entire network, while in the local traffic, the traffic pattern is applied to separate clusters. For the OCI network, there are five clusters corresponding to the five OCI routers. On the other hand, the 64 nodes of the torus network are divided in the network layer into five clusters according to the proximity of the routers. The experiment is conducted by subjecting the NoCs to different traffic patterns for 500 clock cycles each, the latency per packet is then computed by dividing the total number of clock cycles (500) by the total number of packets arrived successfully to their target PEs in each traffic pattern.

Additionally, the throughput Θ is calculated as follows:

$$\Theta = \frac{N_c \times N_b \times N_p}{t_c} \quad (11)$$

where N_c is the number of the simulation clock cycles (500), N_b is the number of bits per packet (256), N_p is the number of packets received by the target PEs, and t_c is the clock period.

As illustrated by Fig. 7(a), the latency in clock cycles per packet of the T-OCI is higher than that of the CONNECT NoC in most traffic patterns due to the serial spreading of packets. However, the latency is lower in the hotspot traffic pattern due to the smaller number of hops needed to reach the hotspot node. Additionally, the P-OCI NoC offers lower packet latency compared with the CONNECT NoC for all traffic patterns except for the uniform pattern since torus NoCs are better in balancing the injected load than star NoCs. Consequently, the P-OCI throughput shown in Fig. 7(b) is higher than that of the CONNECT NoC for all traffic patterns due to its lower clock period. Moreover, the improvement in throughput and area of the T-OCI and P-OCI over those of the CONNECT NoC appears in the throughput-to-area ratio (TPA) comparison in Fig. 7(c). However, as illustrated in Fig. 7(d), the dynamic and static power consumption of the OCI-based NoC for all traffic patterns are larger than that of the CONNECT NoC except the uniform pattern despite the P-OCI's higher clock period. Therefore, the improvement in the TPA of the T-OCI and P-OCI routers comes at the expense of increasing power consumption. Resource replication and adapting the clock speed can be employed to enhance the power consumption.

VI. Conclusion

In this paper, we introduced the concept of overloaded CDMA crossbars as the physical layer enabler of NoC routers. In overloaded CDMA, the communication channel is overloaded with nonorthogonal codes to increase the channel capacity. Two crossbar architectures that leverage the overloaded CDMA concept, namely, T-OCI and P-OCI, are advanced to increase the CDMA crossbar capacity by 100% and $2N \times 100\%$, respectively, where N is the spreading code length. We exploited featured properties of the Walsh spreading code family employed in the classical CDMA crossbar to increase the number of router ports sharing the crossbar without altering the simple accumulator decoder architecture of the conventional CDMA crossbar. Generation procedures of nonorthogonal spreading codes are presented along with the reference and pipelined architectures for each crossbar variant. The T-/P-OCI crossbars were implemented and validated on a Xilinx Artix-7 AC701 FPGA evaluation kit.

The performance of the OCI crossbars is compared with that of the conventional CDMA crossbar. The dynamic power is reduced by 45% for the T-OCI crossbar but increased by 133% for the P-OCI crossbar. The T-OCI crossbar utilizes 31% fewer resources, while the P-OCI crossbar uses 400% more resources compared with the conventional CDMA crossbar. The OCI crossbar suitability for NoCs has been established by analytically and experimentally evaluating a fully working OCI-based NoC. A 65-node OCI-based star NoC was realized and compared with an SDMA-based torus NoC generated by CONNECT. The evaluation results demonstrate the superiority of the OCI-based NoCs in terms of area and throughput.

Many future work directions are inspired by this paper including exploiting the mathematical properties of the code space to find additional nonorthogonal codes and boost the CDMA interconnect capacity and exploring more architectural optimizations of the OCI crossbar. Studying the robustness of CDMA interconnects and its enhancement techniques will be one of the prior future research points. Moreover, we plan to investigate using the OCI-based routers in different network topologies, evaluate their performance using standard benchmarks, and study their suitability for various applications.

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