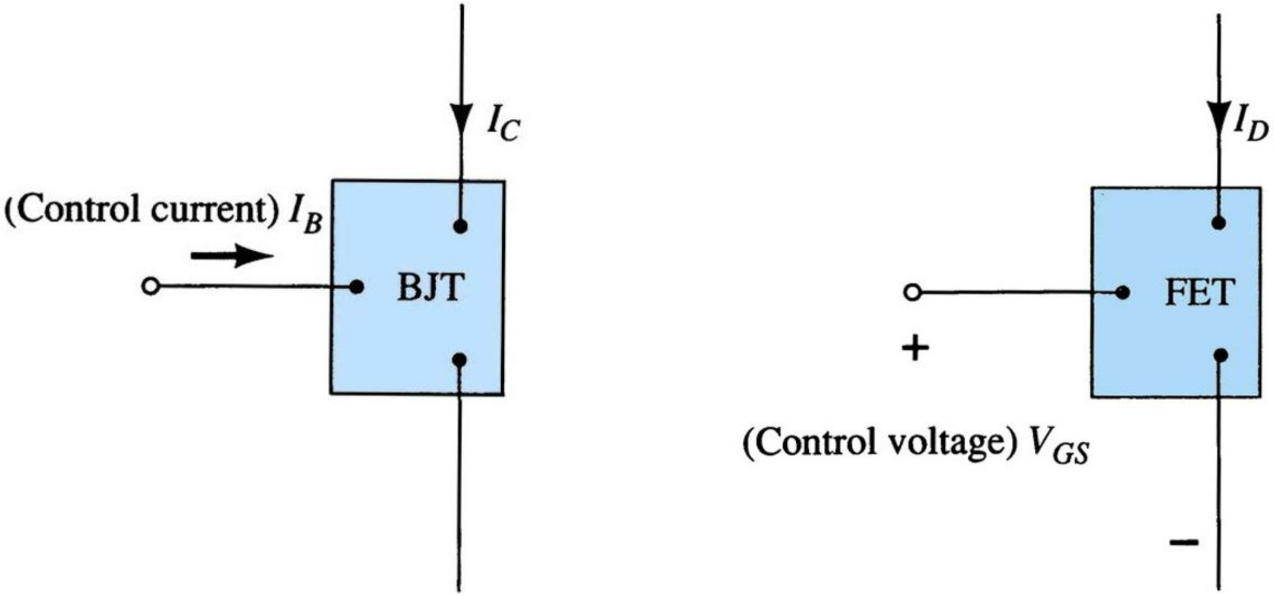
Field-Effect Transistor (FET)

Introduction

- Field-effect means that an electric field is established by the charges present, which controls the conduction path of the output circuit without the need to direct contact between the controlling and controlled quantities
- FET is a voltage-controlled device while BJT is a current-controlled device

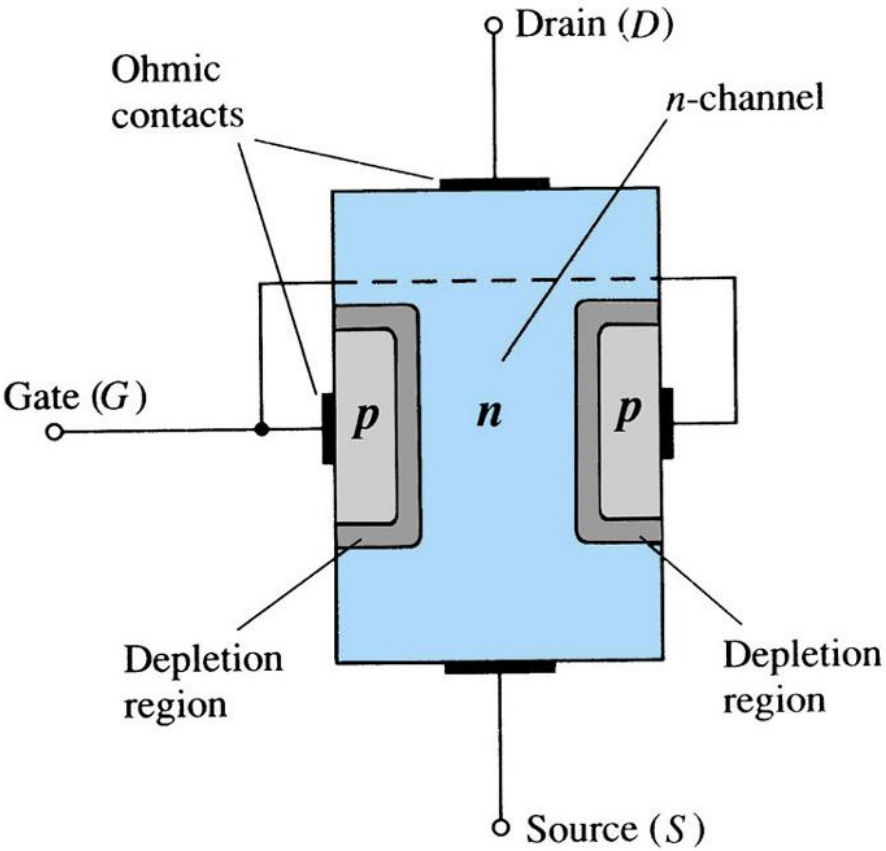


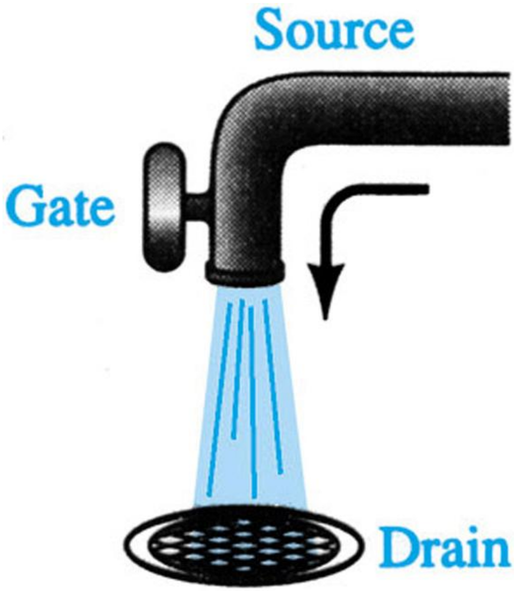
Introduction

- FET are more temperature stable than BJT
- FET are smaller than BJT, making them suitable for IC chips
- 2 types of FET will be introduced:
  - Junction Field-Effect Transistor (JFET)
  - Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

Construction of JFET

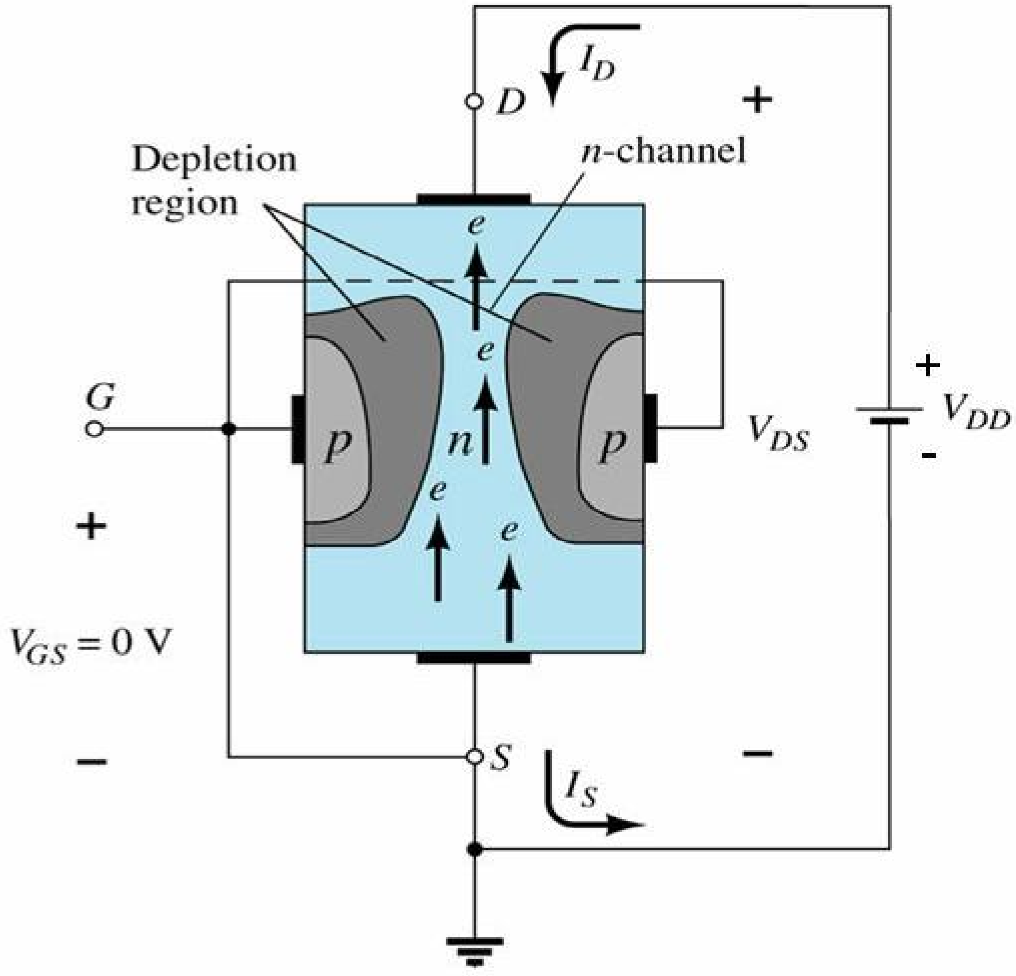
- For n-channel JFET:





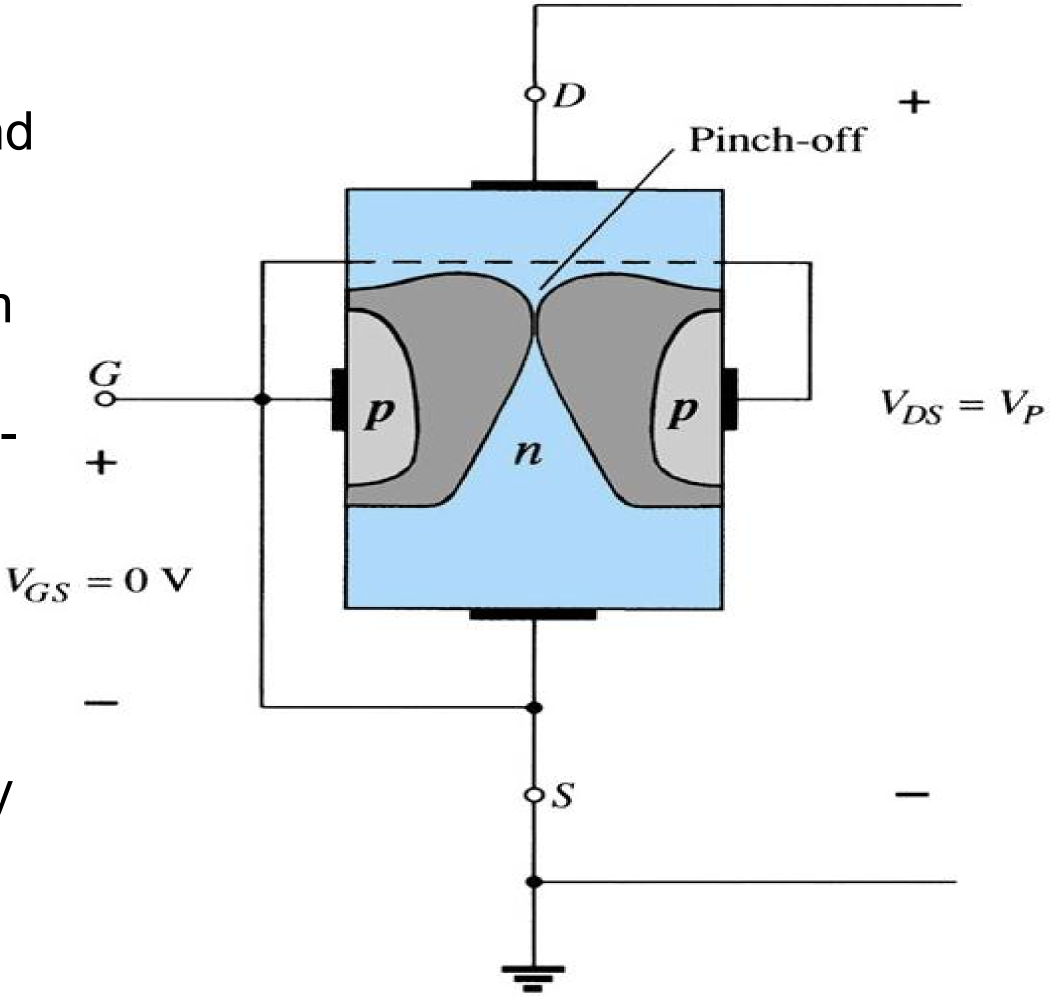
Characteristics of JFET

- By applying voltage at the JFET's terminal (V_{GS} = 0 V and V_{DS} = +ve values), some characteristic can be obtained
- For the n-type material, electrons will be attracted to the positive terminal of V_{DS}
- For the p-type material at gate, holes will be attracted to the negative terminal and further away from the positive terminal of V_{DS}
- As for that, depletion region will become larger between the n-type and p-type materials
- Resistance will increase due to narrowing channel



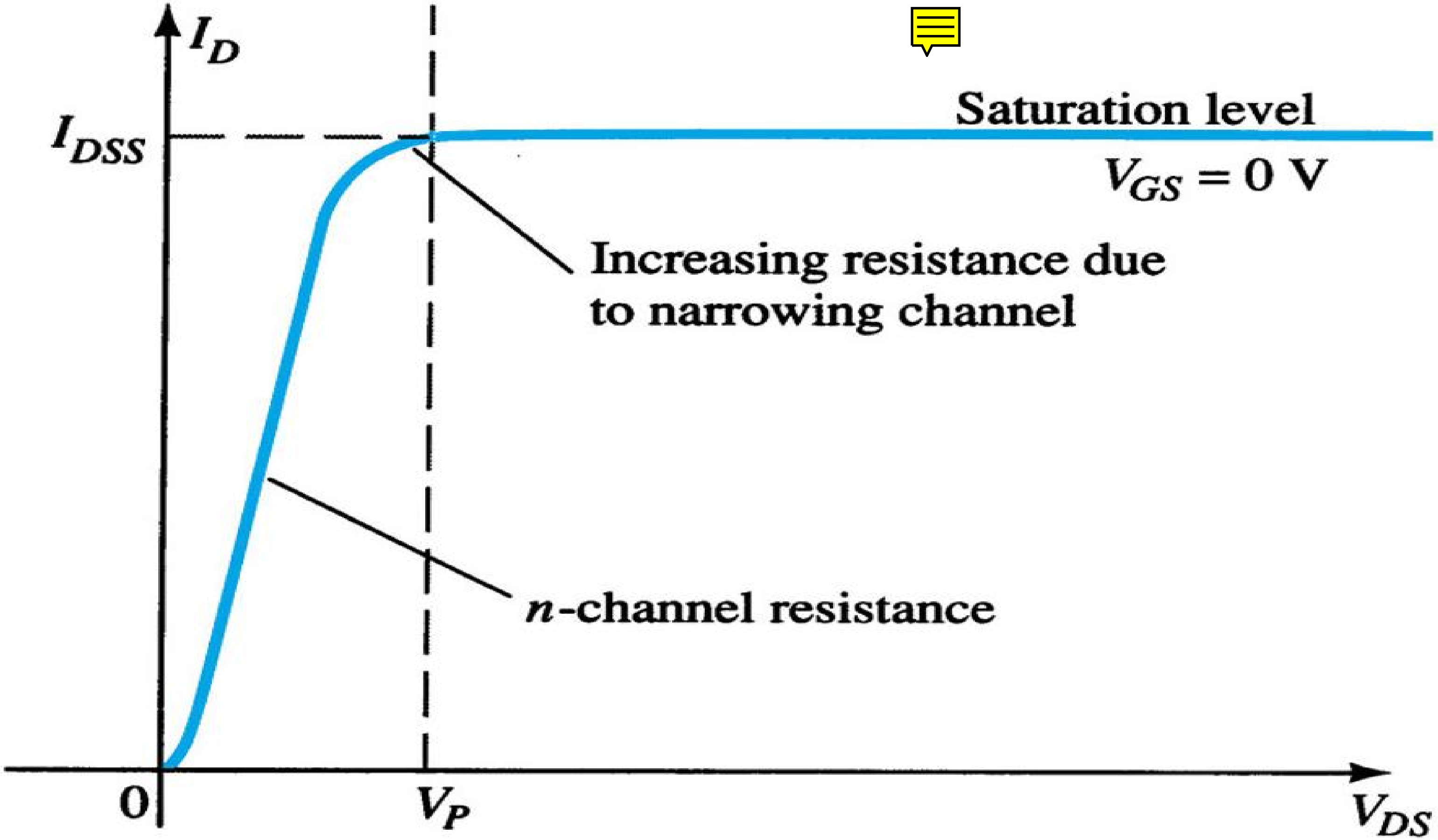
Characteristics of JFET

- When the +ve value of V_{DS} is increased, the depletion regions will become larger and such that it seems to be touching each other and blocks the electron flows from source to drain
- The condition is called "pinch-off" and the voltage at that point is called "pinch-off voltage (V_P)"
- But in reality, a very small channel still exist and current can flow through it with a very high density – the current (I_D) is maintained at saturation level (I_{DDS})



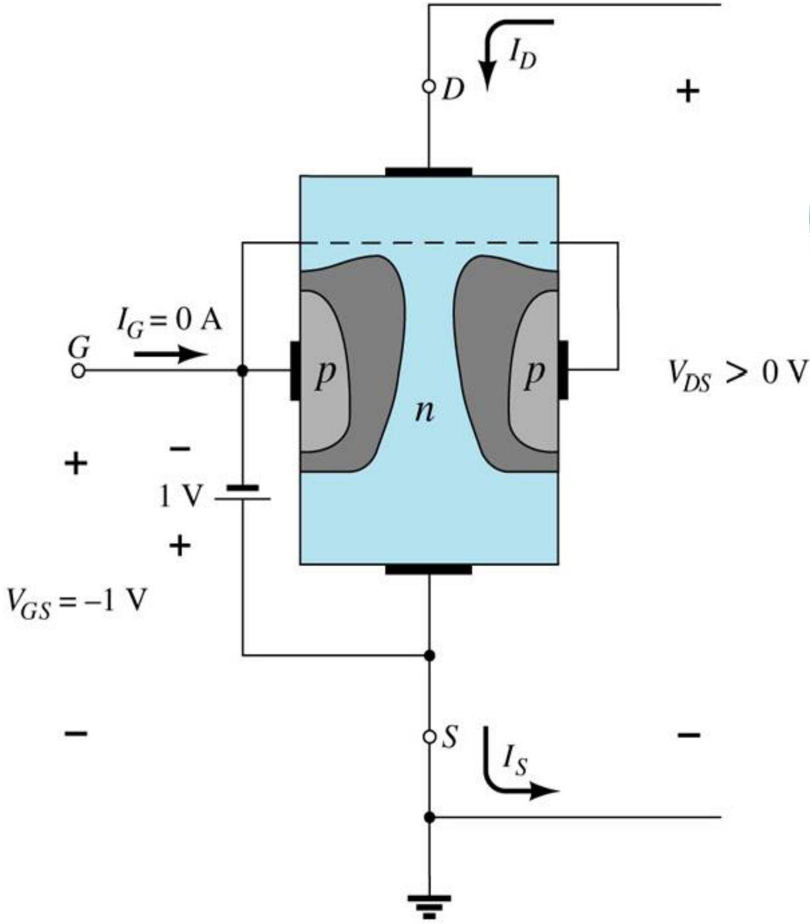
Characteristics of JFET

- From the experiment above, the characteristic below will be obtained:

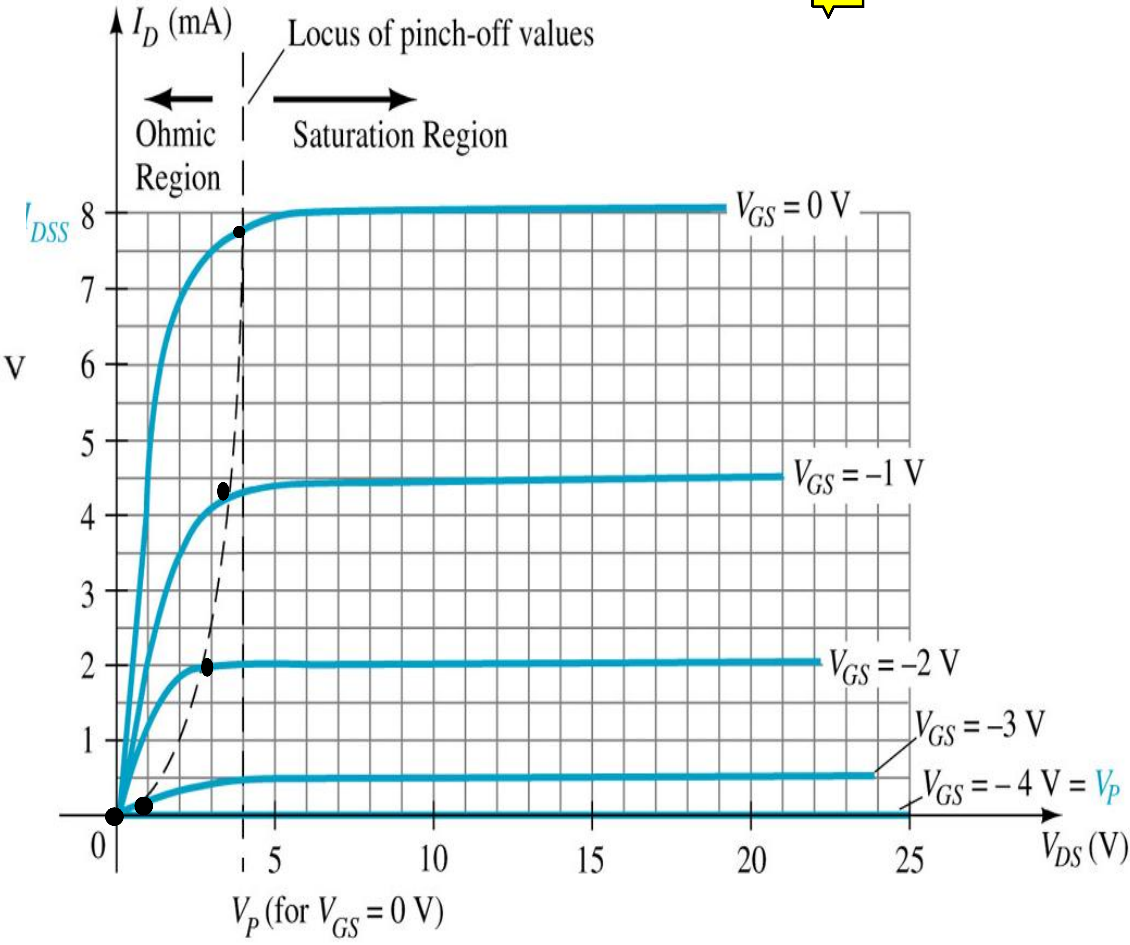


Characteristics of JFET

- For $V_{GS} < 0$ V:

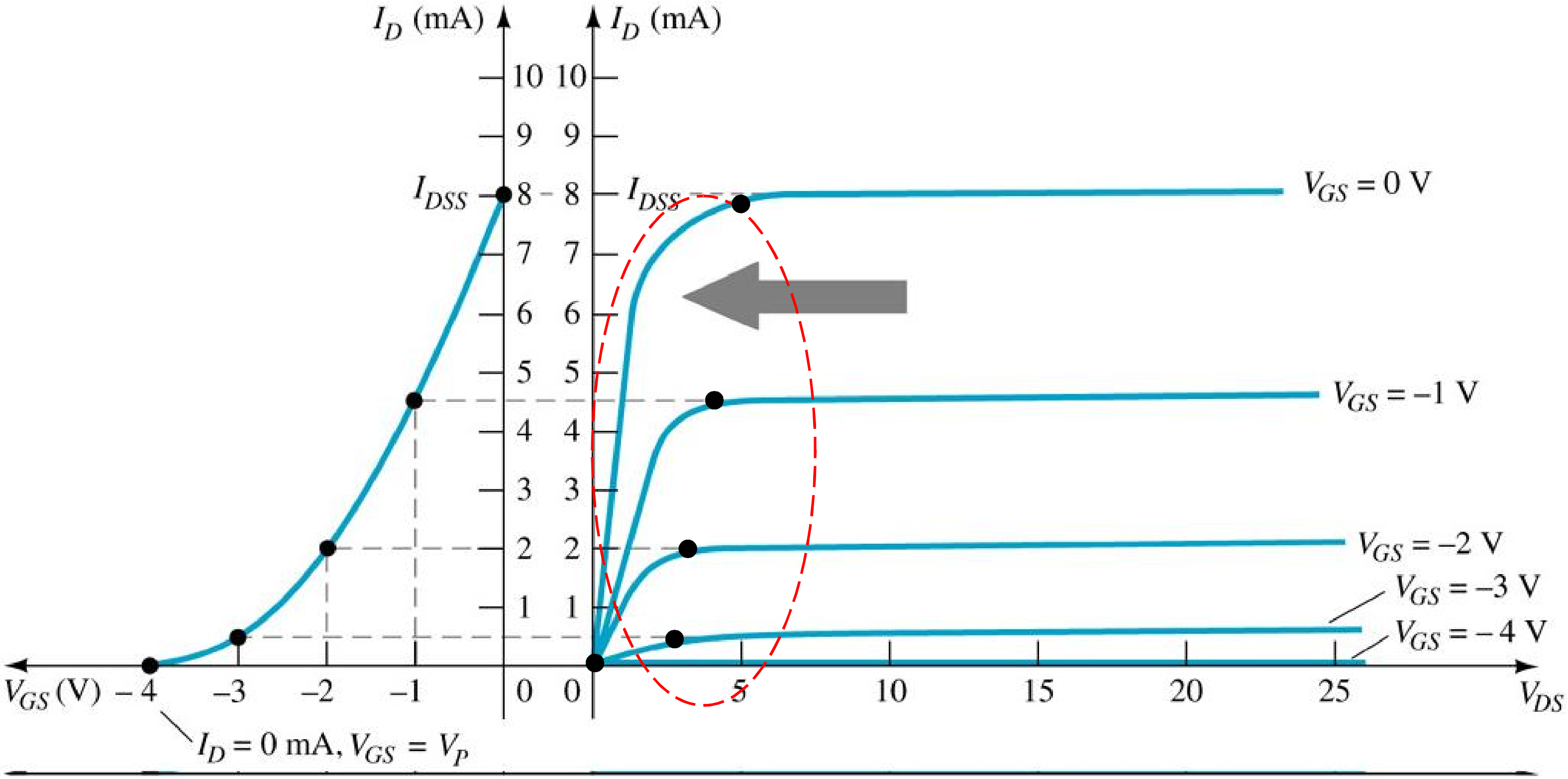


- The characteristic obtained:



Transfer Characteristic of JFET

- But for JFET characteristic, V_P in the circled region is said to be drop in a parabolic manner



Transfer Characteristic of JFET

- As for that, the linear equation just like in BJT characteristic cannot be applied
- However, Shockley's equation can be applied for that region resulting in:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

- where I_{DSS} – current drain to source at saturation level

  V_{GS} – voltage from gate to source

  V_P – pinch-off voltage

Plotting Shockley's Equation

- V_{GS} and I_D points can be plotted using this table:

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0

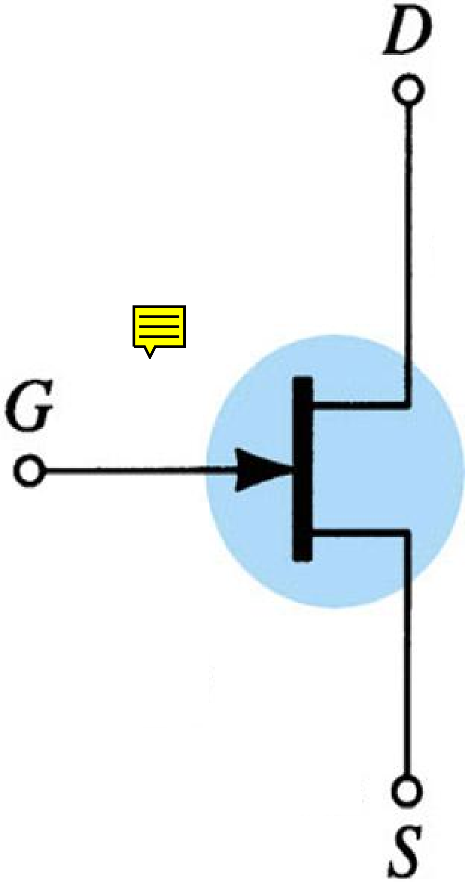
n-channel JFET Symbols

- For *n*-channel JFET:

$$I_G = 0$$

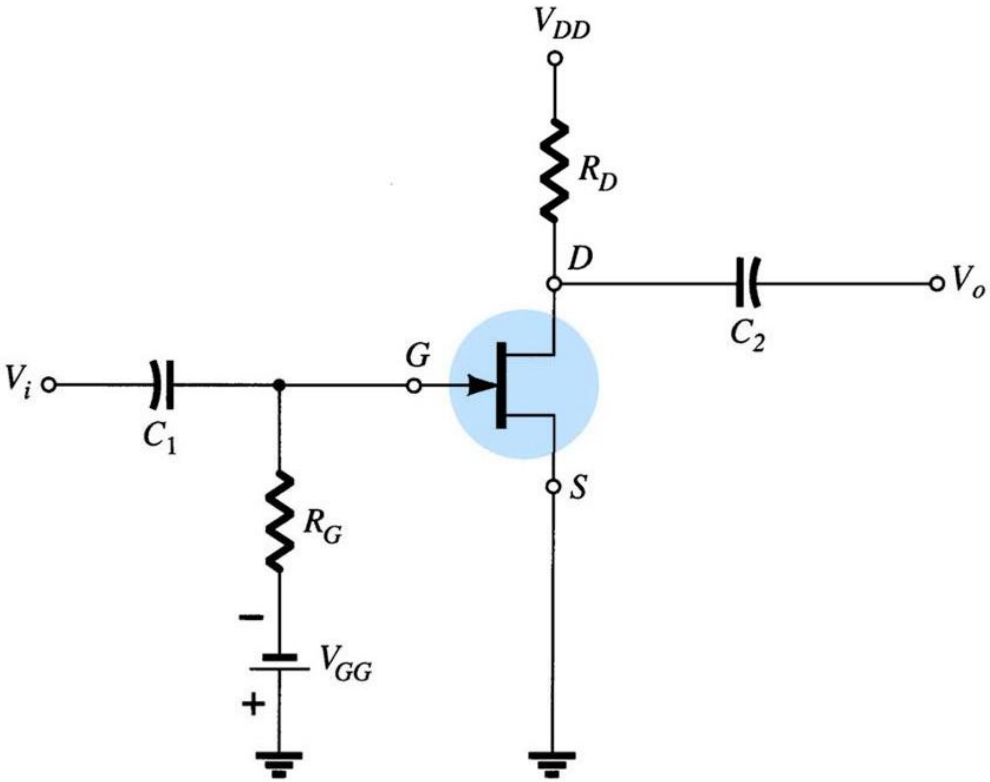
$$I_D = I_S$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$



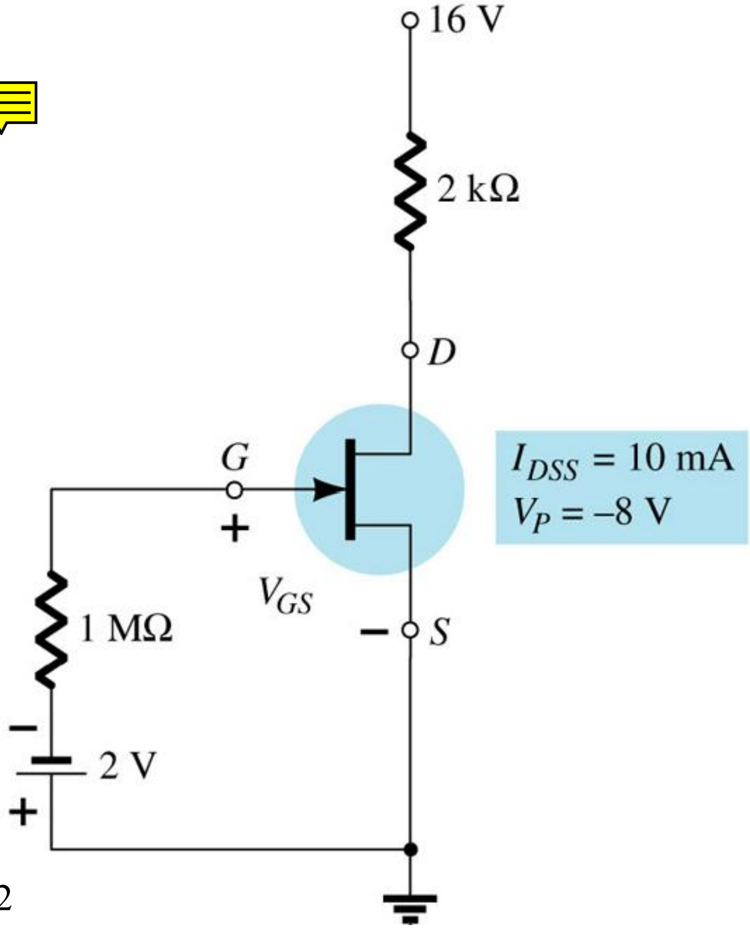
Fixed-Bias Configuration

- Recall back from BJT’s topic, for fixed-bias configuration emitter terminal is grounded. Same for FET’s fixed-bias configuration:



Example 7.1

- Determine:
  - V_{GSQ} , I_{DQ}
  - V_{DS} , V_D , V_G , V_S



When $I_G = 0$, $V_G = -2$ V
Due to source terminal is grounded, so $V_S = 0$ V
V_{GS} can be obtained:

$$V_{GS} = V_G - V_S = -2 - 0 = -2\text{ V}$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10m\left(1 - \frac{-2}{-8}\right)^2 = 5.625\text{ mA}$$

Example 7.1

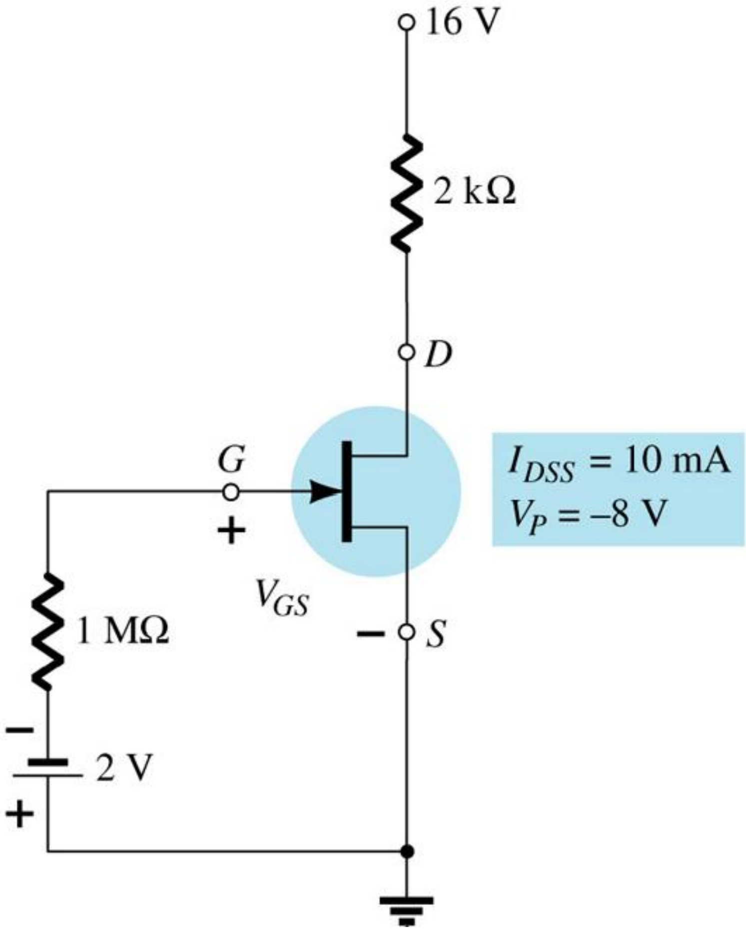
- For V_{DS}:

$$V_{DS} = V_D - V_S = V_D - 0 = V_D$$

$$V_D = V_{DD} - I_D R_D$$

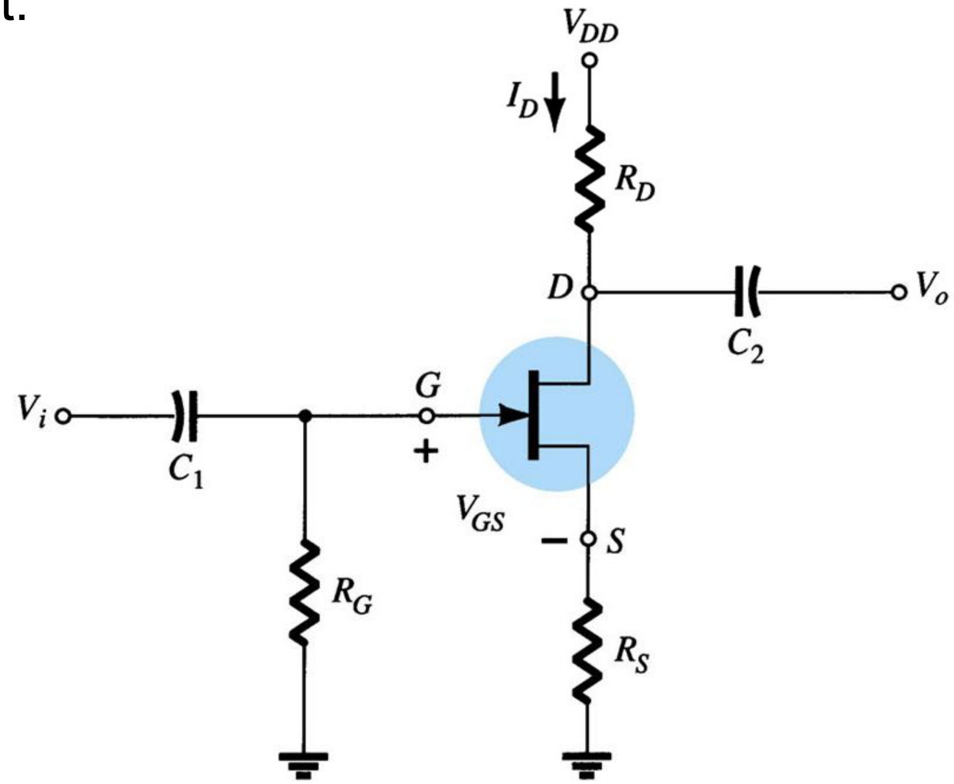
$$= 16 - 5.625\text{mA} * 2\text{k}\Omega = 4.75\ \text{V}$$

$$\therefore V_{DS} = V_D = 4.75\ \text{V}$$



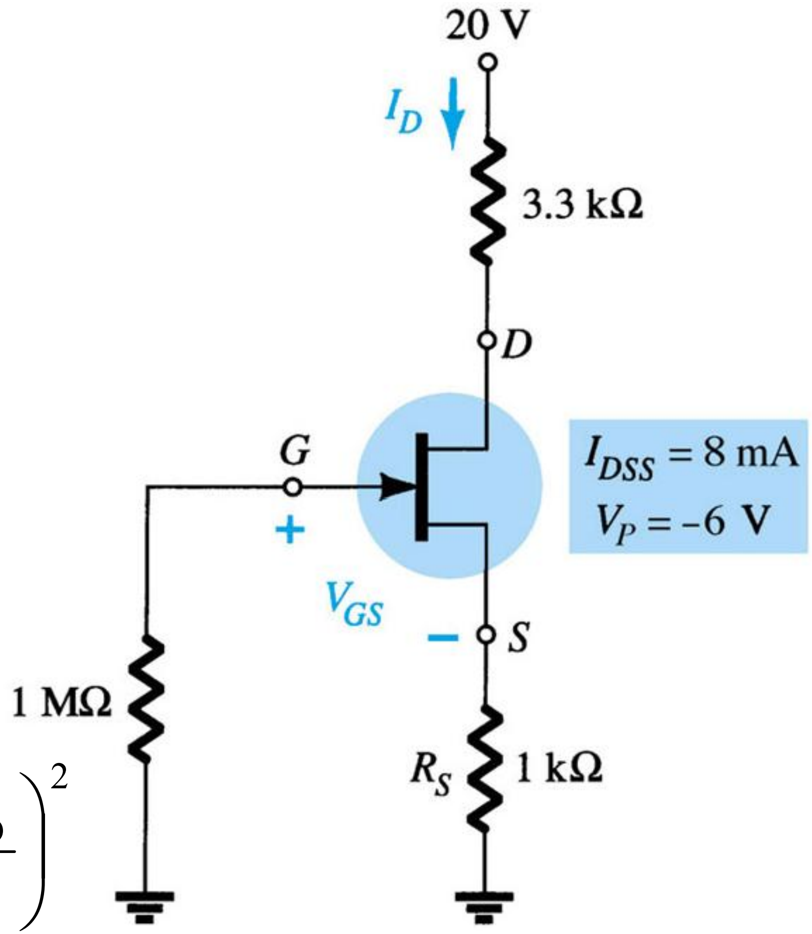
Self-Bias Configuration

- Self-bias configuration was introduced to eliminate the need for 2 DC supplies and a resistor was added at source terminal
- The circuit:



Example 7.2

- Determine:
  - V_{GSQ} , I_{DQ} ,V_{DS} ,V_D , V_G ,V_S



$$I_S = I_D = \frac{V_S}{R_S} = \frac{V_S}{1k}$$

$$\therefore V_S = 1kI_D$$

$$V_{GS} = V_G - V_S = 0 - 1kI_D = -1kI_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8m\left(1 - \frac{-1kI_D}{-6}\right)^2$$

$$\therefore 222.24I_D^{\,2} - 3.67I_D + 8m = 0$$

Example 7.2

- Solving the equation, we get:

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{3.67 \pm \sqrt{(-3.67)^2 - 4(222.24)(8m)}}{2(222.24)}$$

$$= 13.93 \text{ mA and } 2.58 \text{ mA}$$

- I_D = 2.58 mA is taken due to I_D = 13.93 mA is out of range because the maximum value of I_D is I_{DSS} which is 8 mA
- When the value of I_D has been obtained, all the other value can be calculated easily

Example 7.2

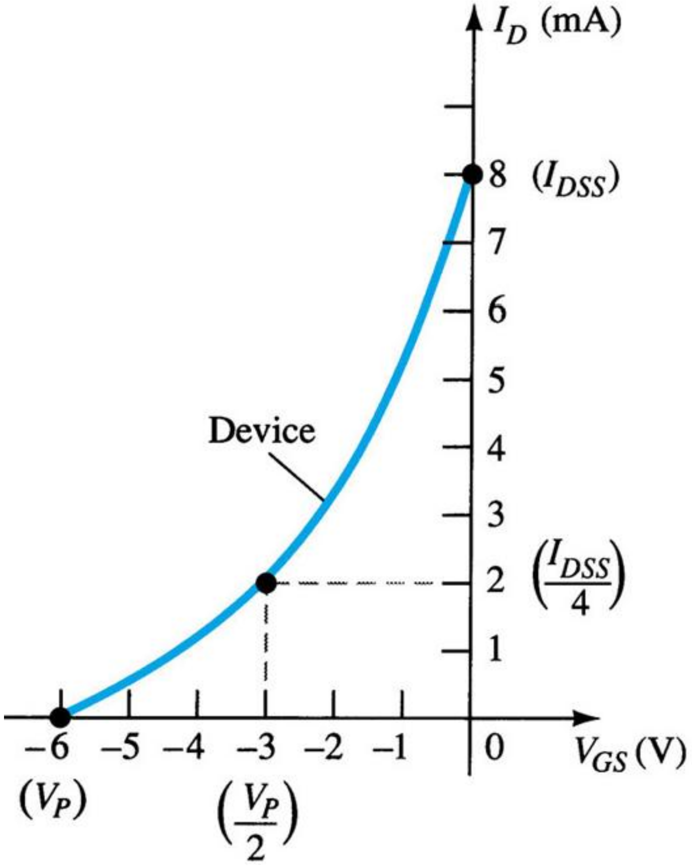
- Using the graphical approach to get the Shockley's curve:

V_{GS}	I_{DD}
0 V	I_{DSS} = 8 mA
$0.3V_P$ = -1.8 V	$I_{DSS}/2$ = 4 mA
$0.5V_P$ = -3 V	$I_{DSS}/4$ = 2 mA
V_P = -6 V	0 mA

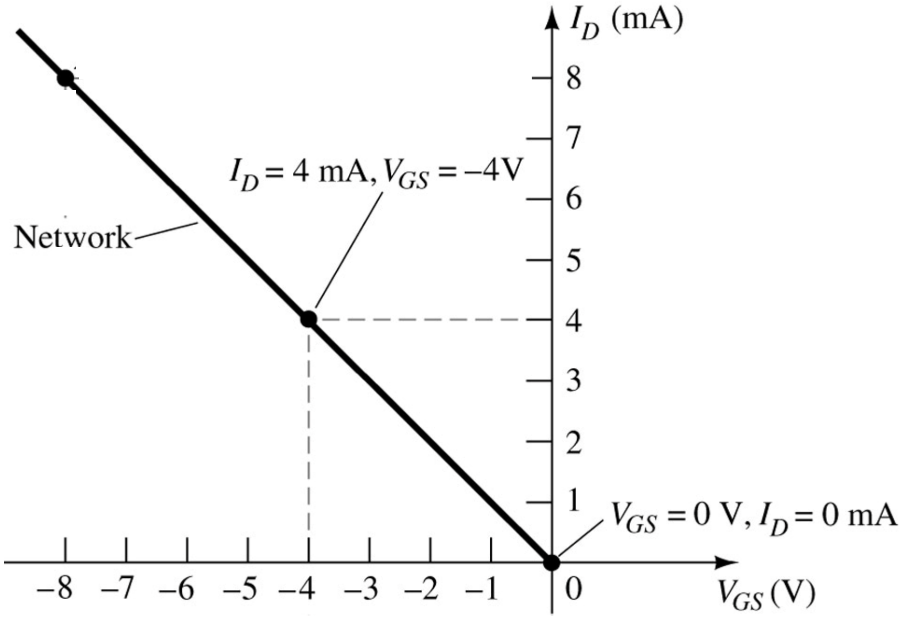
- From the circuit, equation of V_{GS} is: $V_{GS} = -1kI_D$
- Take two points for plotting:
  - If I_D = 0 A, V_{GS} = 0 V ➔ (0,0)
  - If I_D = 4 mA, V_{GS} = -4 V ➔ (-4,4m)

Example 7.2

- Shockley's curve:

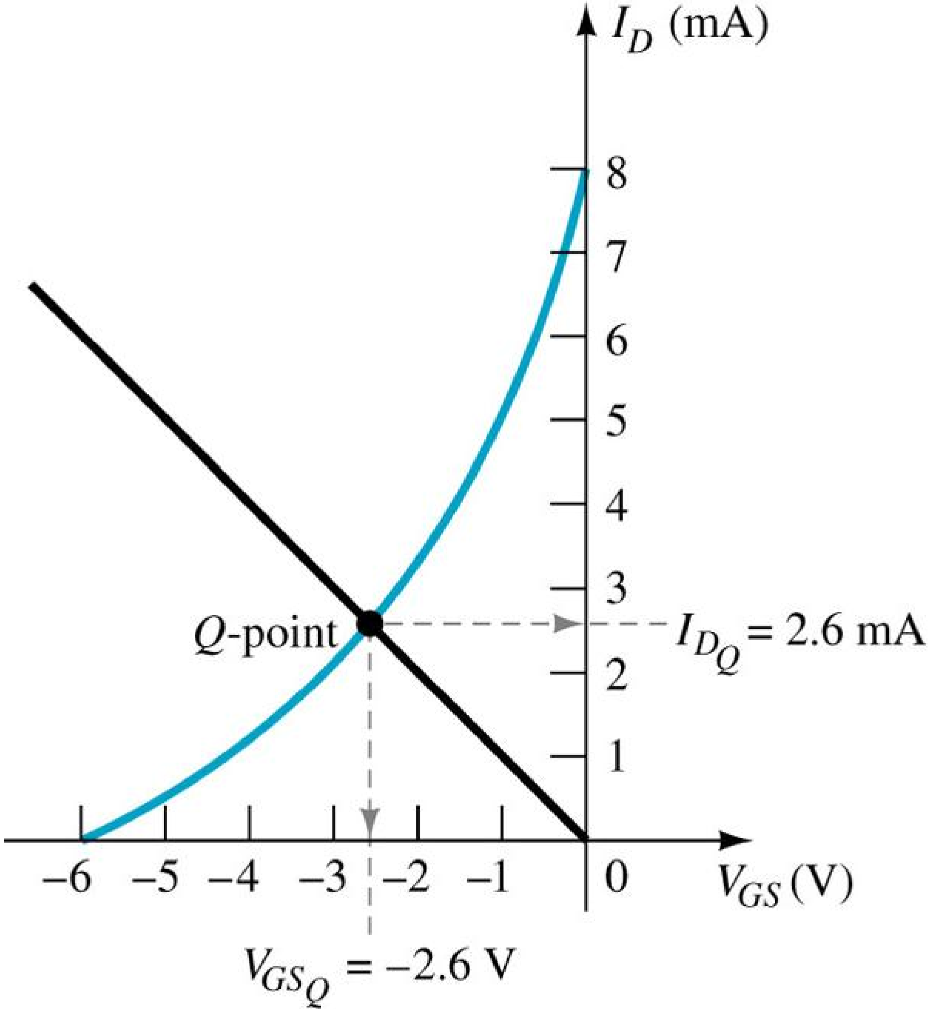


- V_{GS} equation from the circuit:



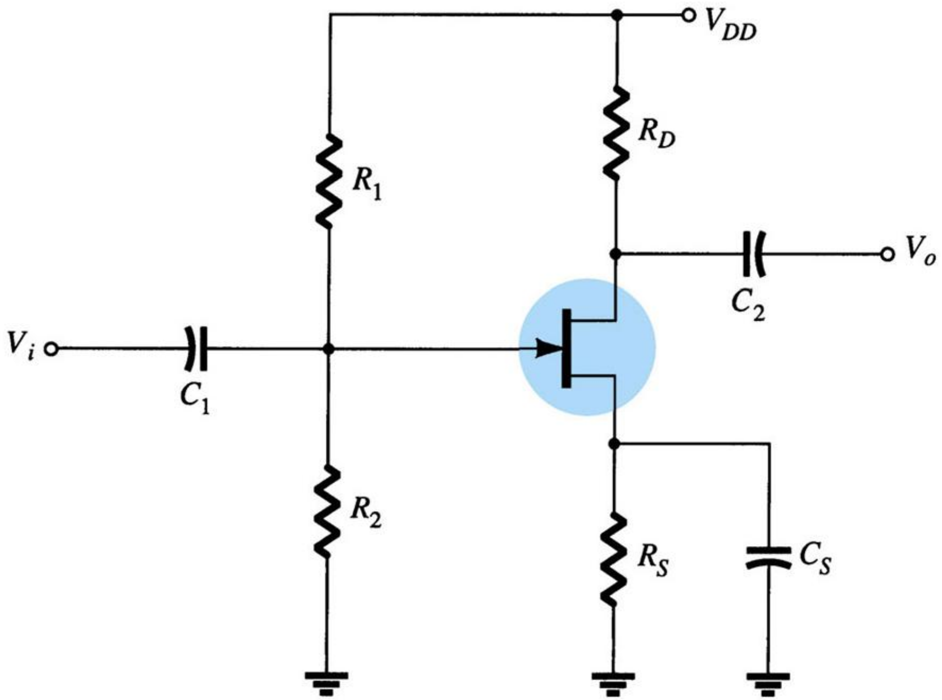
Example 7.2

- Combining the Shockley's curve and V_{GS} equation of the circuit:
- The Q-point is at $I_D = 2.6$ mA which is very close to the value of I_D obtained by using mathematical approach
- All the other value can be obtained just as the same as in mathematical approach

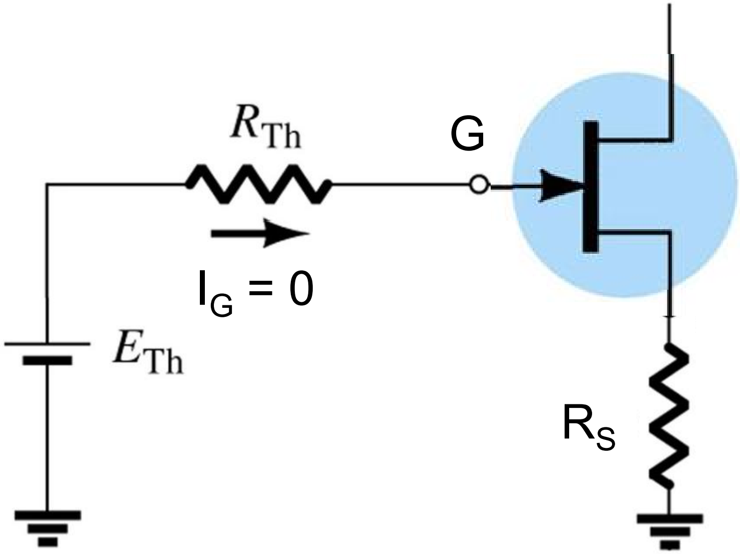


Voltage-Divider Bias Configuration

- The circuit:



- Gate terminal equivalent:



For $I_G = 0$, so $V_G = E_{TH}$, no need to calculate R_{TH} value

Example 7.5

- First, calculate V_G:

$$V_G = 16 * \frac{270\,\text{k}}{270\,\text{k} + 2.1\text{M}} = 1.82\text{ V}$$

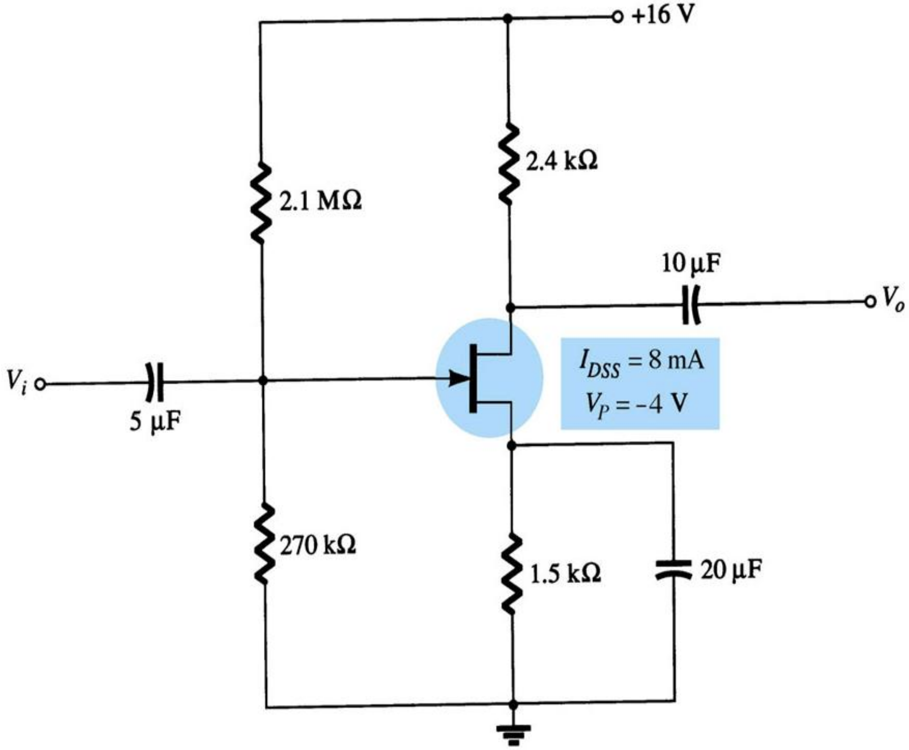
- For V_S:

$$I_S = I_D = \frac{V_S}{R_S} = \frac{V_S}{1.5k}$$

$$\therefore V_S = 1.5kI_D$$

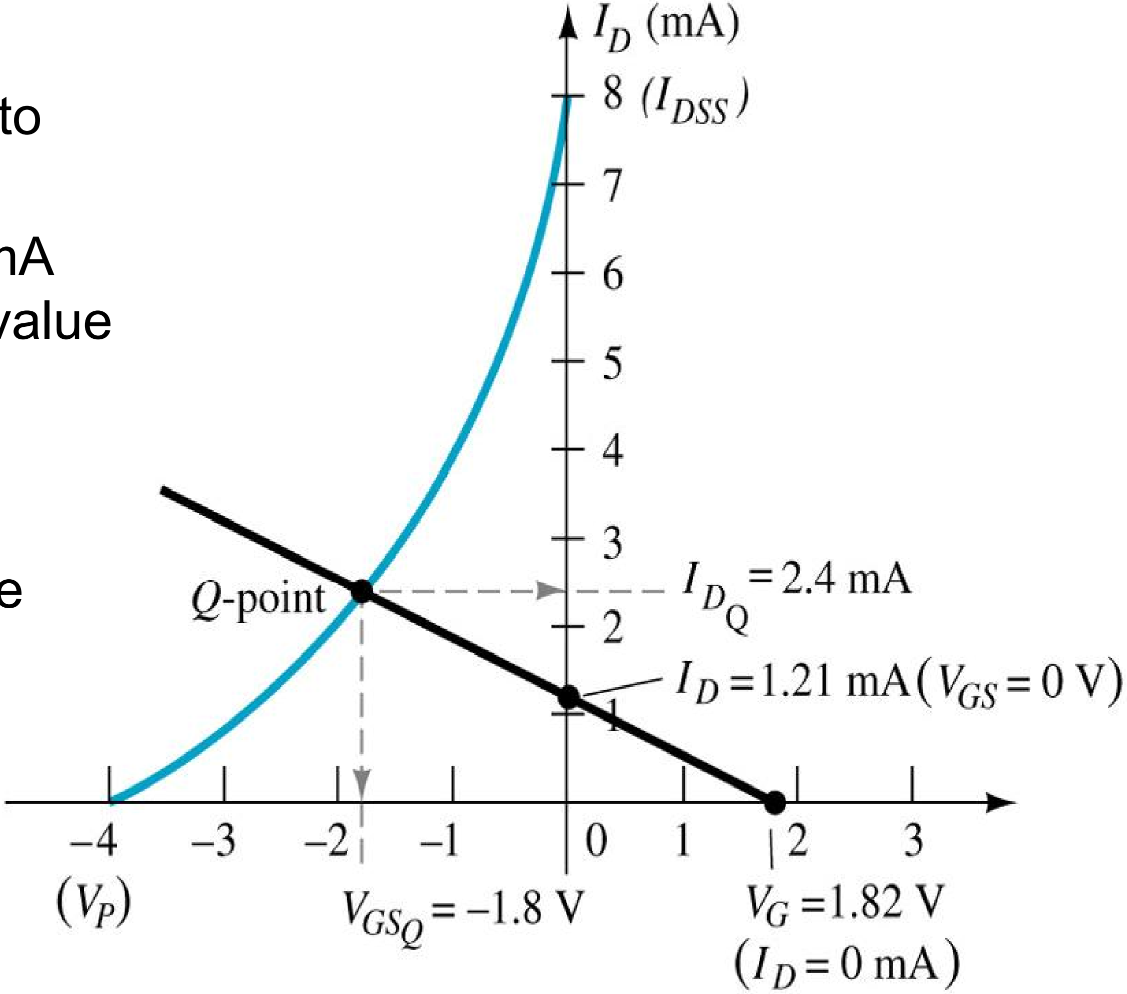
- So, for V_{GS}:

$$V_{GS} = V_G - V_S = 1.82 - 1.5kI_D$$



Example 7.5

- Using graphical approach to confirm the value of I_{DQ}:
- The Q-point is at $I_D \approx 2.4$ mA which is very close to the value of I_D obtained by using mathematical approach
- All the other value can be obtained after obtaining the value of I_D



Example 7.5

- Calculating I_D using Shockley's equation:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 8m\left(1-\frac{1.82-1.5kI_D}{-4}\right)^2$$

$$\therefore 1.13kI_D{}^2 - 9.73I_D + 16.96m = 0$$

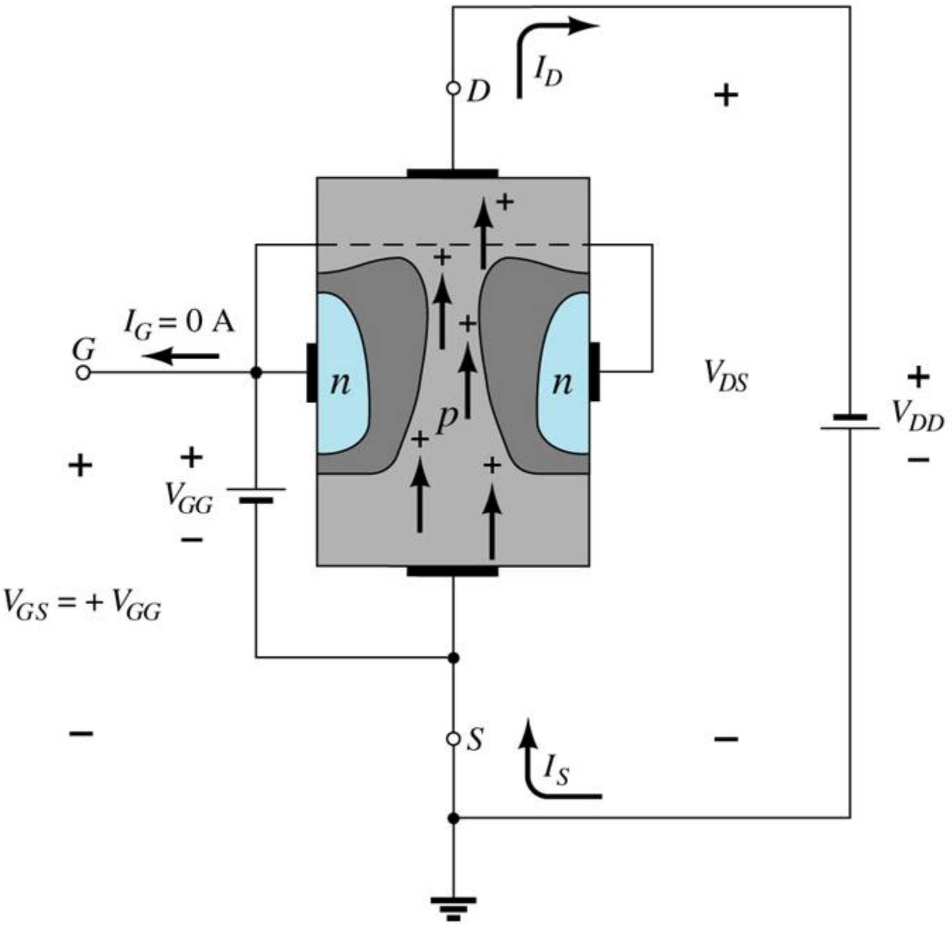
- Solving the equation, we get:

$$I_D = \frac{-b\pm\sqrt{b^2-4ac}}{2a} = \frac{9.73\pm\sqrt{(-9.73)^2-4(1.13k)(16.96m)}}{2(1.13k)}$$

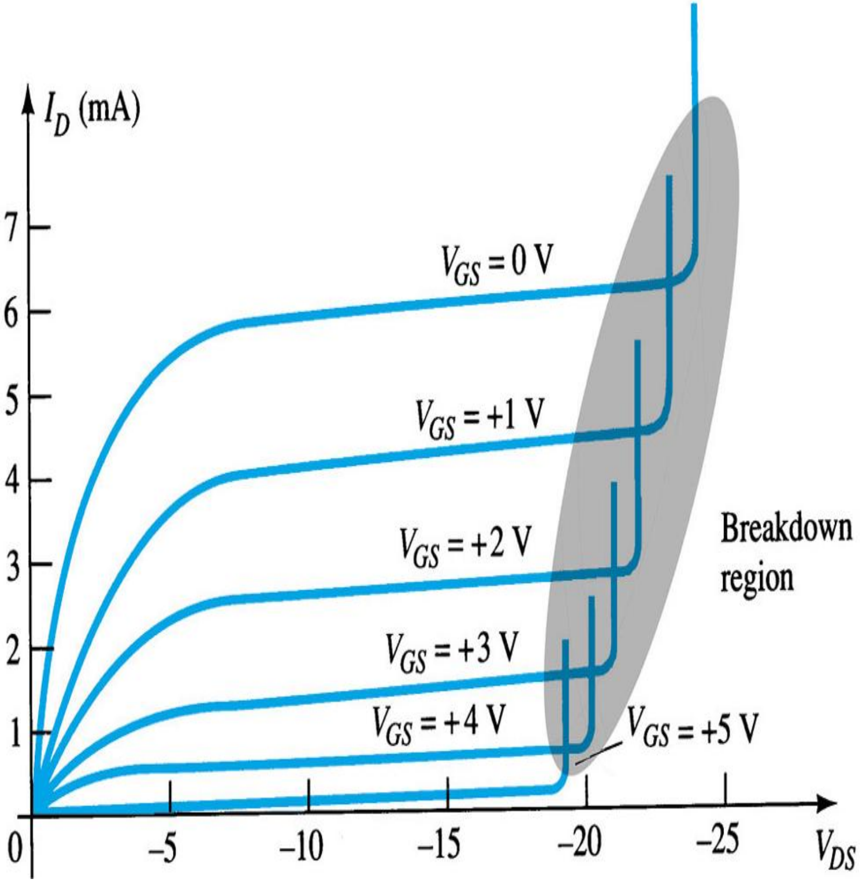
$$= 6.18\,\mathrm{mA}\text{ and }2.43\,\mathrm{mA}$$

p-Channel JFET

- The device:

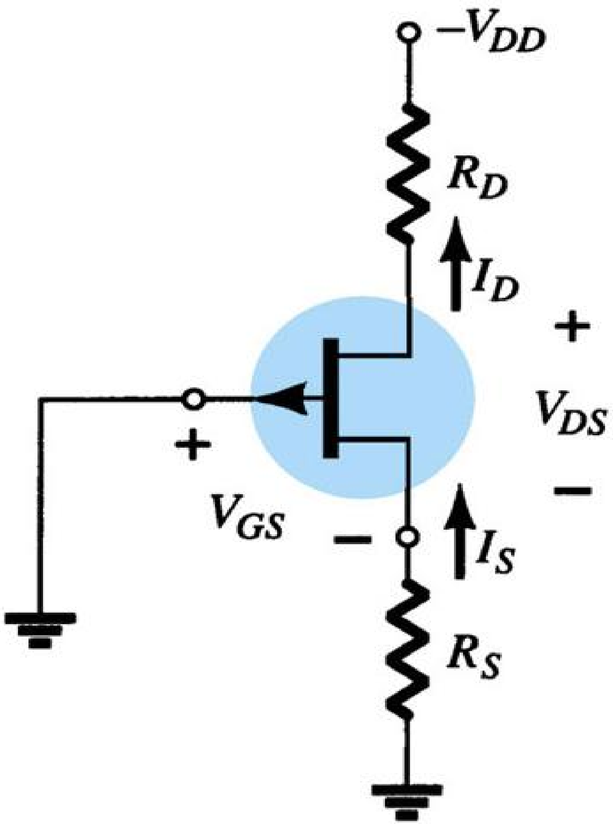


- The characteristic:

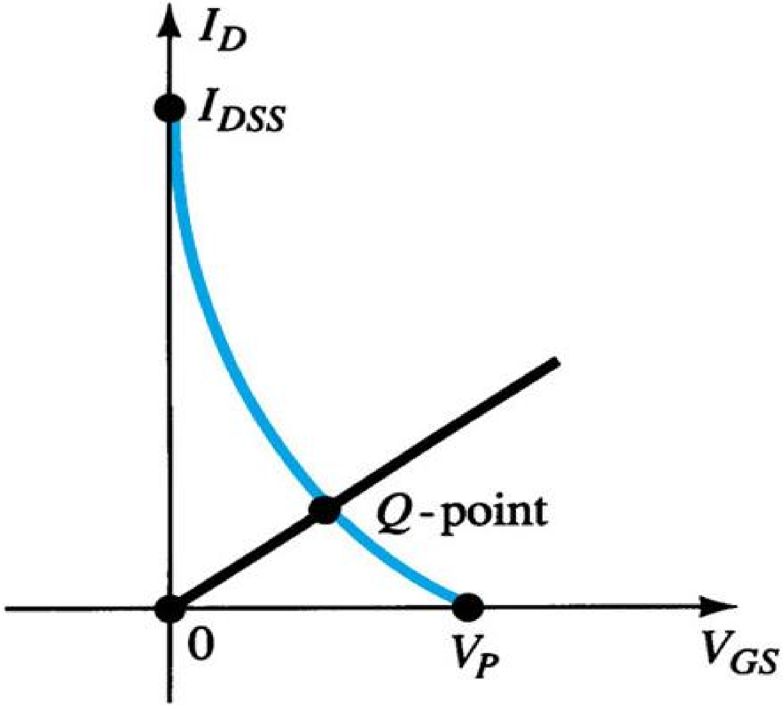


p-channel JFET Configuration and Characteristic (I_D versus V_{GS})

- Configuration:



- Characteristic:

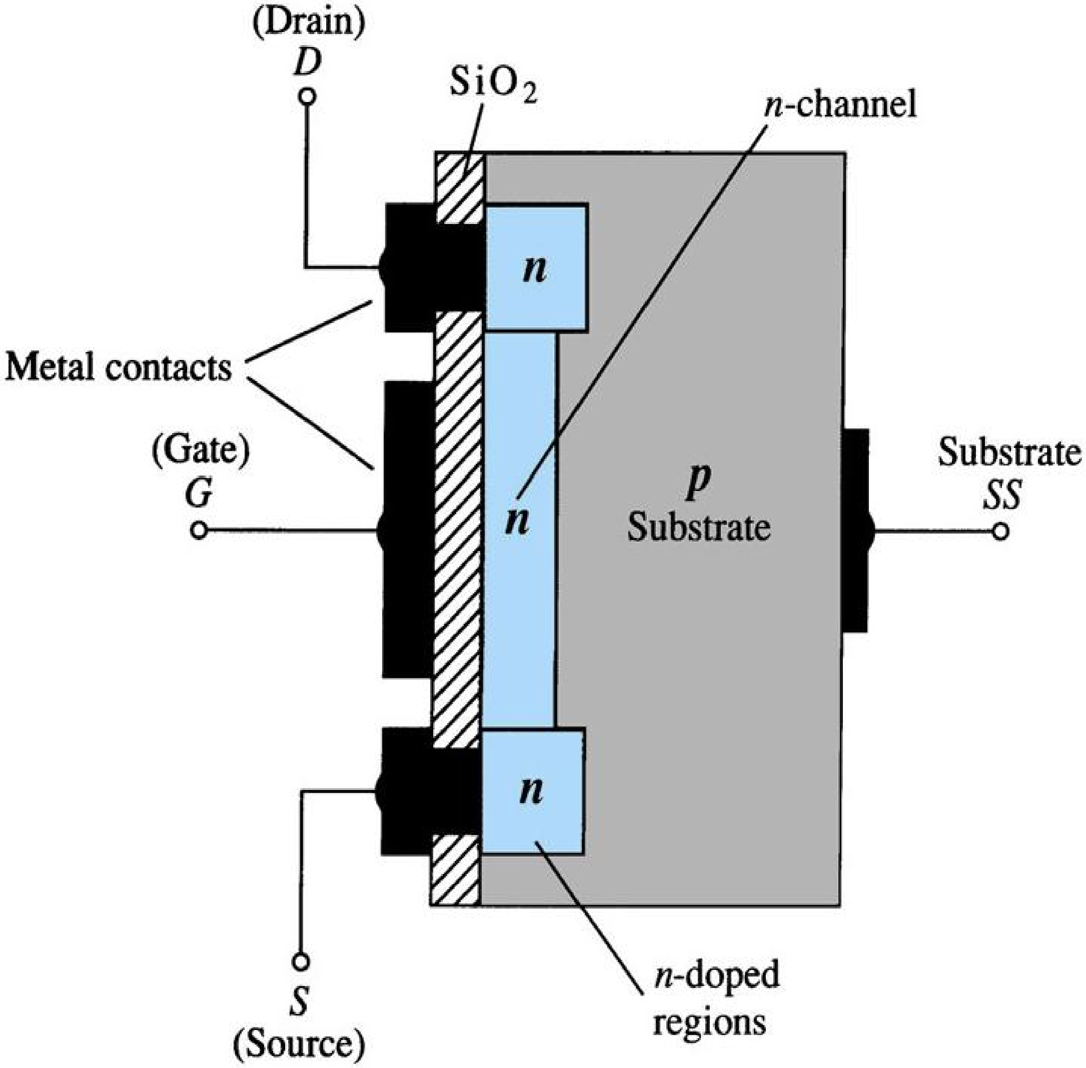


MOSFET

- MOSFET stands for Metal-Oxide Semiconductor Field-Effect Transistor
- Metal-Oxide means there are metal and silicon oxide (SiO_2) involved in its construction
- 2 types of MOSFET:
  - Depletion-Type MOSFET
  - Enhancement-Type MOSFET

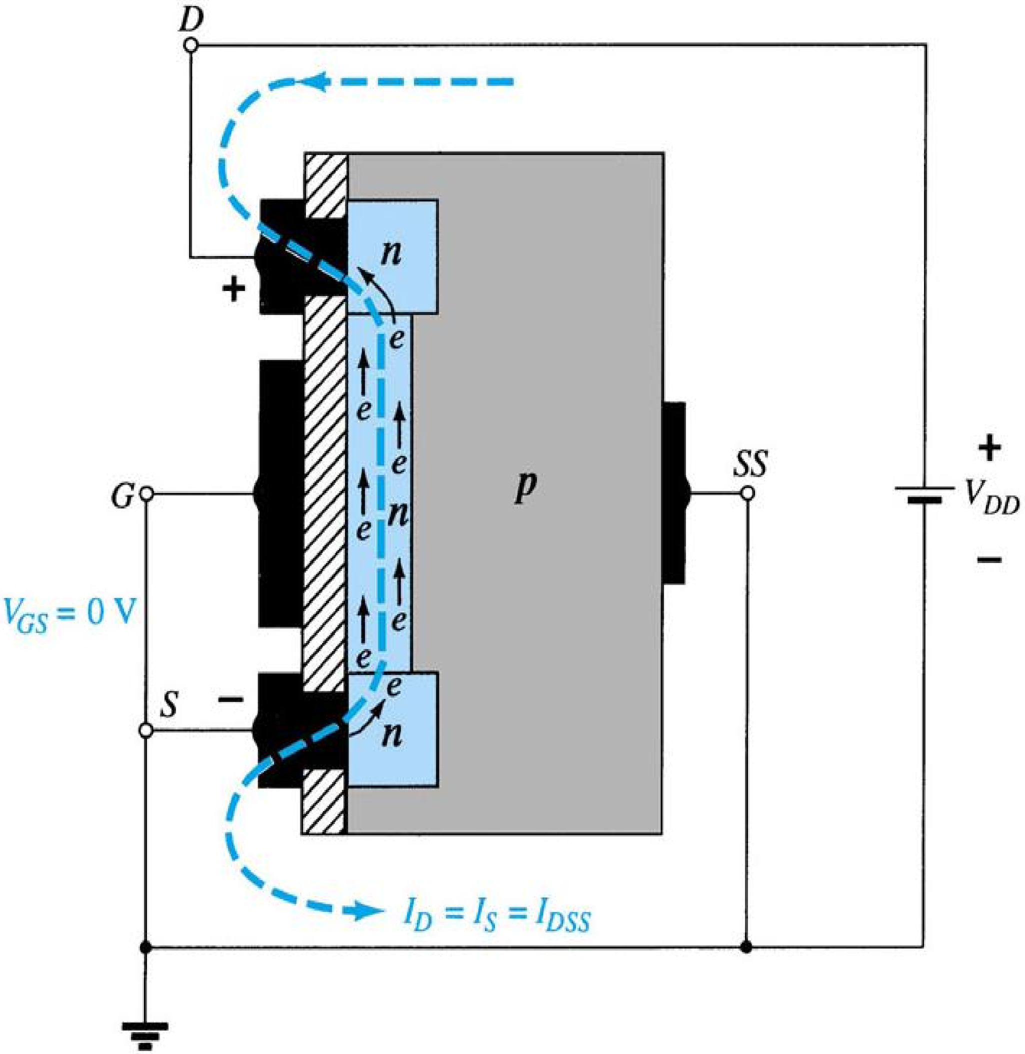
Depletion-Type MOSFET Construction

- *n*-channel depletion-type MOSFET will be discussed first
- The construction is the same with JFET except the addition of SiO_2 under the gate terminal contact and an *n*-channel between two *n*-material



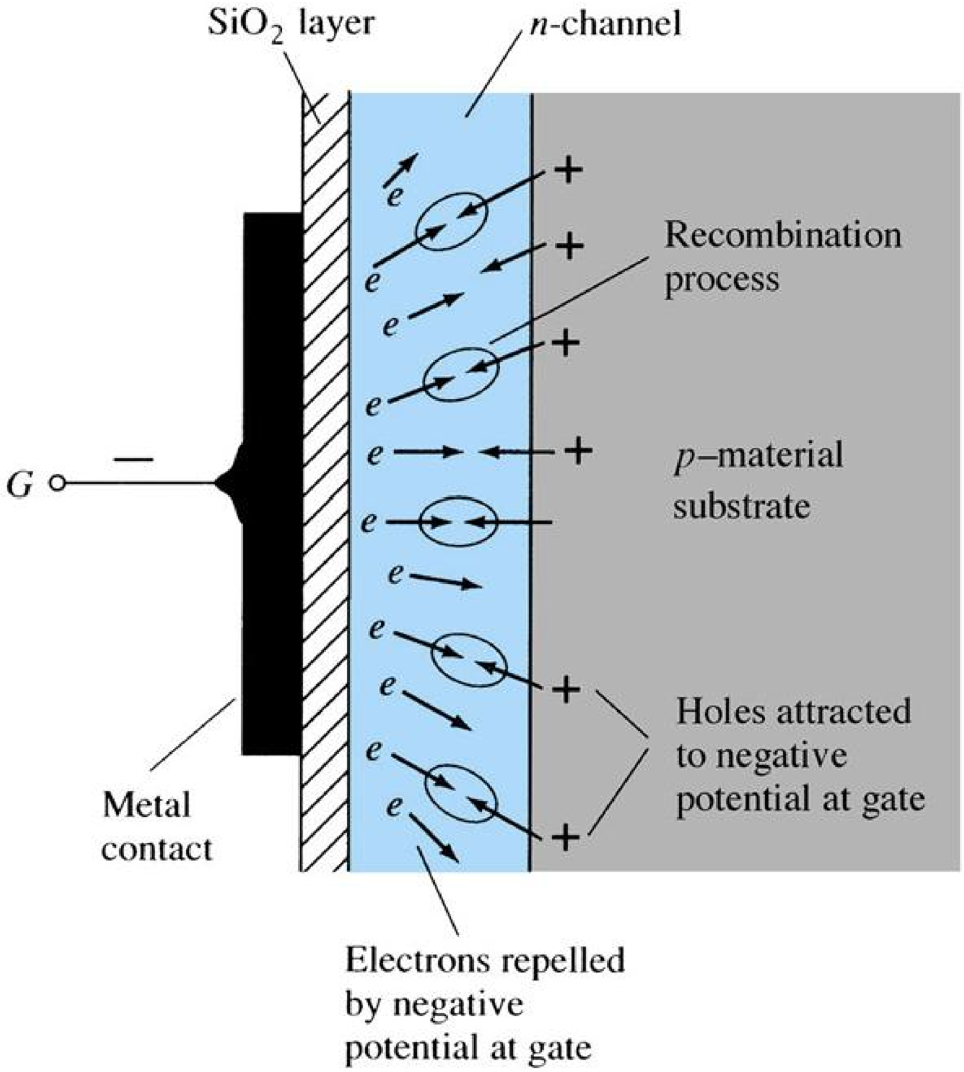
Depletion-Type MOSFET Operation

- Lets apply some positive voltage connected to the drain-source terminal while remaining the gate voltage to 0
- Electrons will flow from source to drain and this will result in current flows from drain to source
- The result will be the same as in JFET and saturation current will be obtained when the pinch-off voltage (V_P) is reached



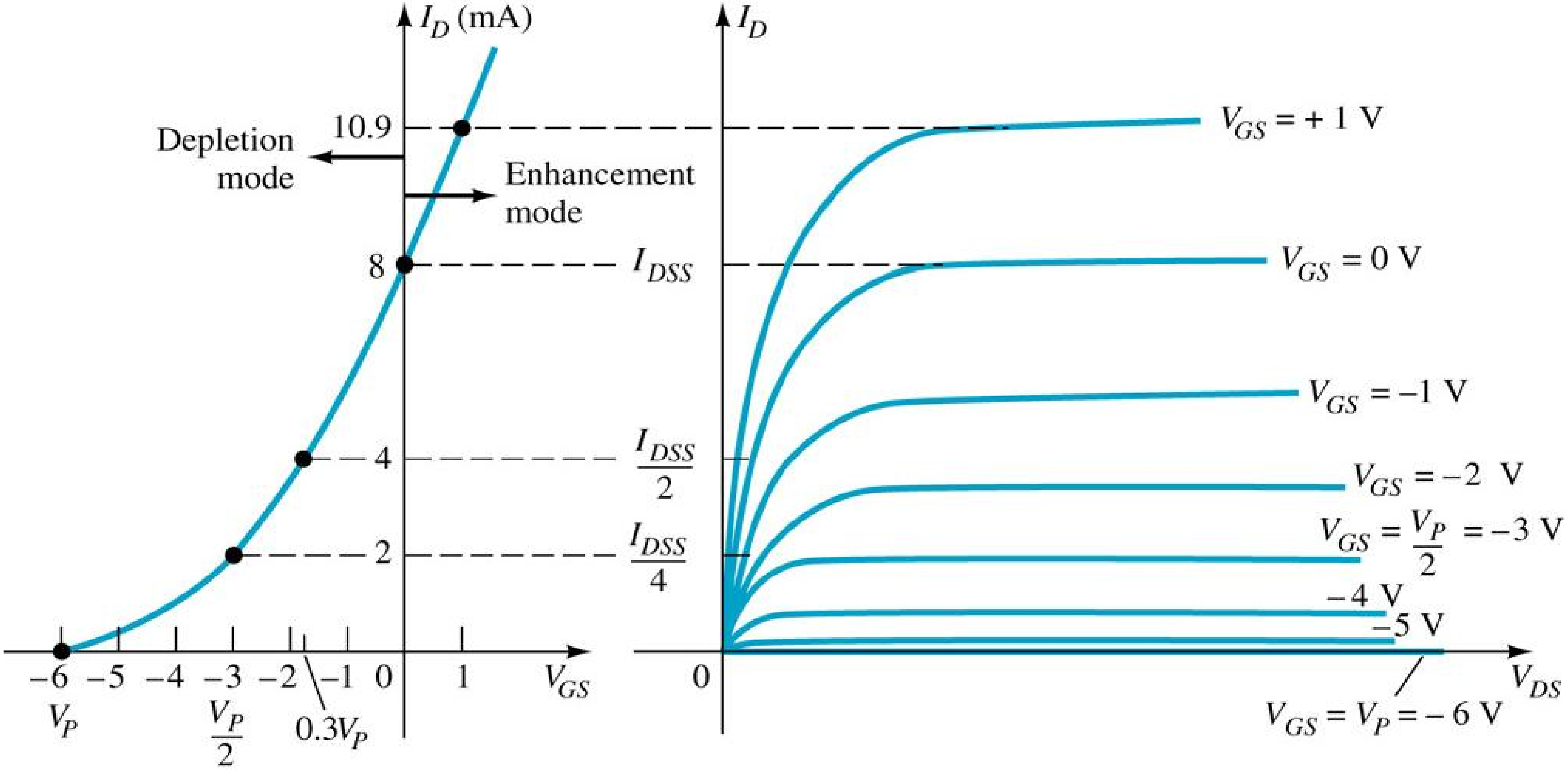
Depletion-Type MOSFET Operation

- Now, lets apply some negative voltage for gate terminal
- The negative voltage will push the electrons in the *n*-channel away from the gate, thus the channel will become smaller
- In addition, the holes in p-material substrate will be attracted to the electrons in the channel and the recombination process will take place, helping the channel to become smaller



Depletion-Type MOSFET Characteristic

- The characteristic:



Depletion-Type MOSFET Characteristic

- As the Shockley's curve applied for the depletion mode, same goes for the enhancement mode
- The Shockley's equation will also be the same, but for the enhancement mode, positive voltage will be applied for V_{GS}
- This will be difference between Depletion-Type MOSFET and JFET characteristic

Example 6.3

- Sketch the transfer curve defined by I_{DSS} = 10 mA and V_P = -4 V
- Obtain the four plot points that is in the depletion region:

V_{GS}	I_D
0 V	10 mA
-1.2 V	5 mA
-2 V	2.5 mA
-4 V	0 mA

Example 6.3

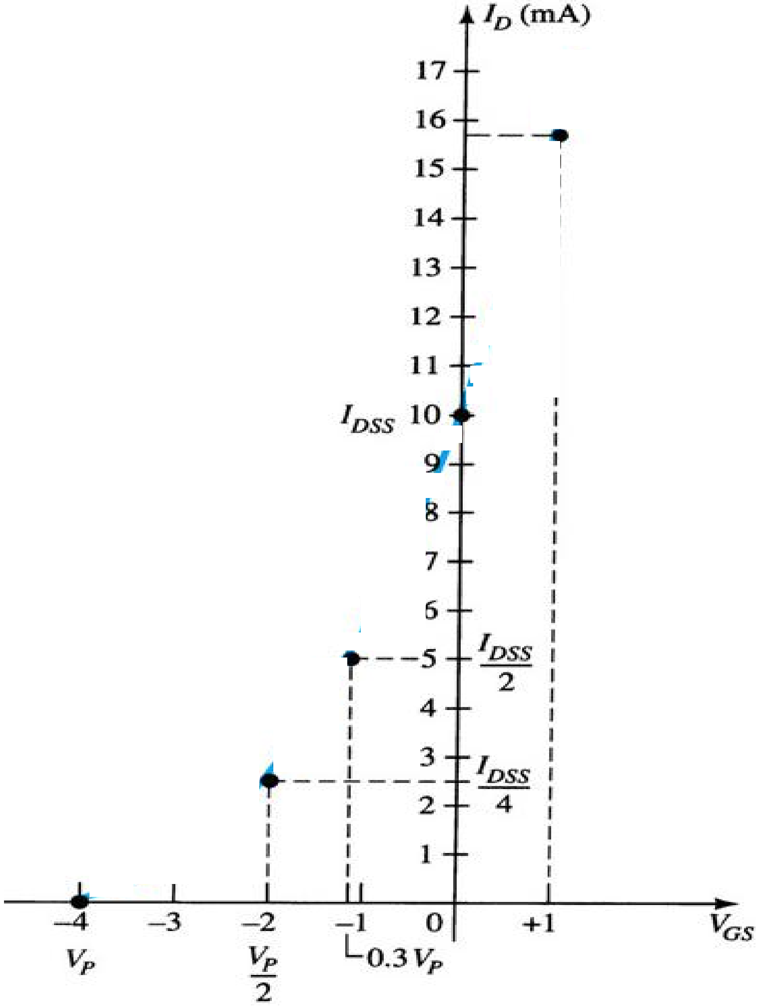
- Obtain the extra plot points that is in the enhancement region (apply V_{GS} = +1 V):

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 10m\left(1-\frac{+1}{-4}\right)^2 = 15.63\,\text{mA}$$

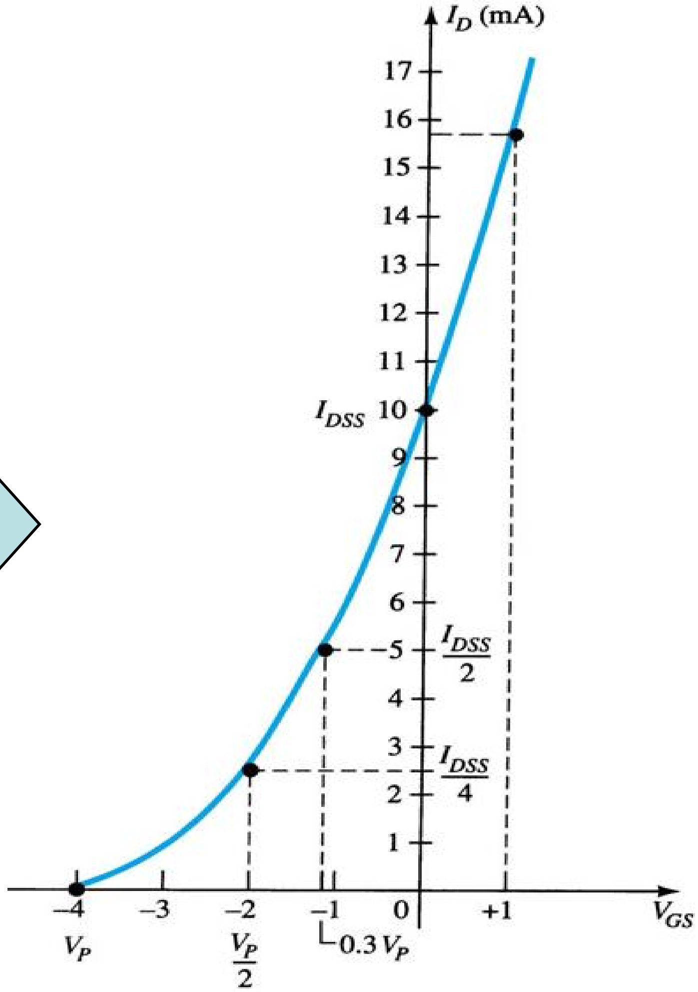
V_{GS}	I_D
+1 V	15.63 mA

Example 6.3

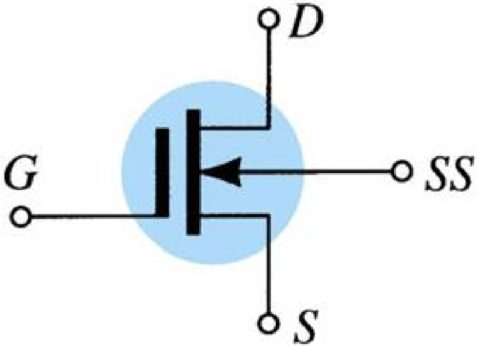
- Plotting:



- Sketching:



n-channel Depletion-Type MOSFET Symbols



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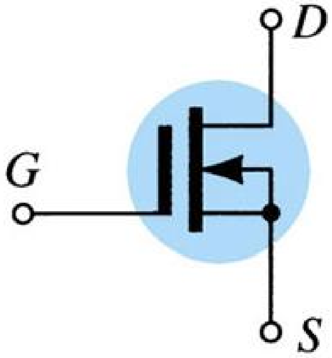
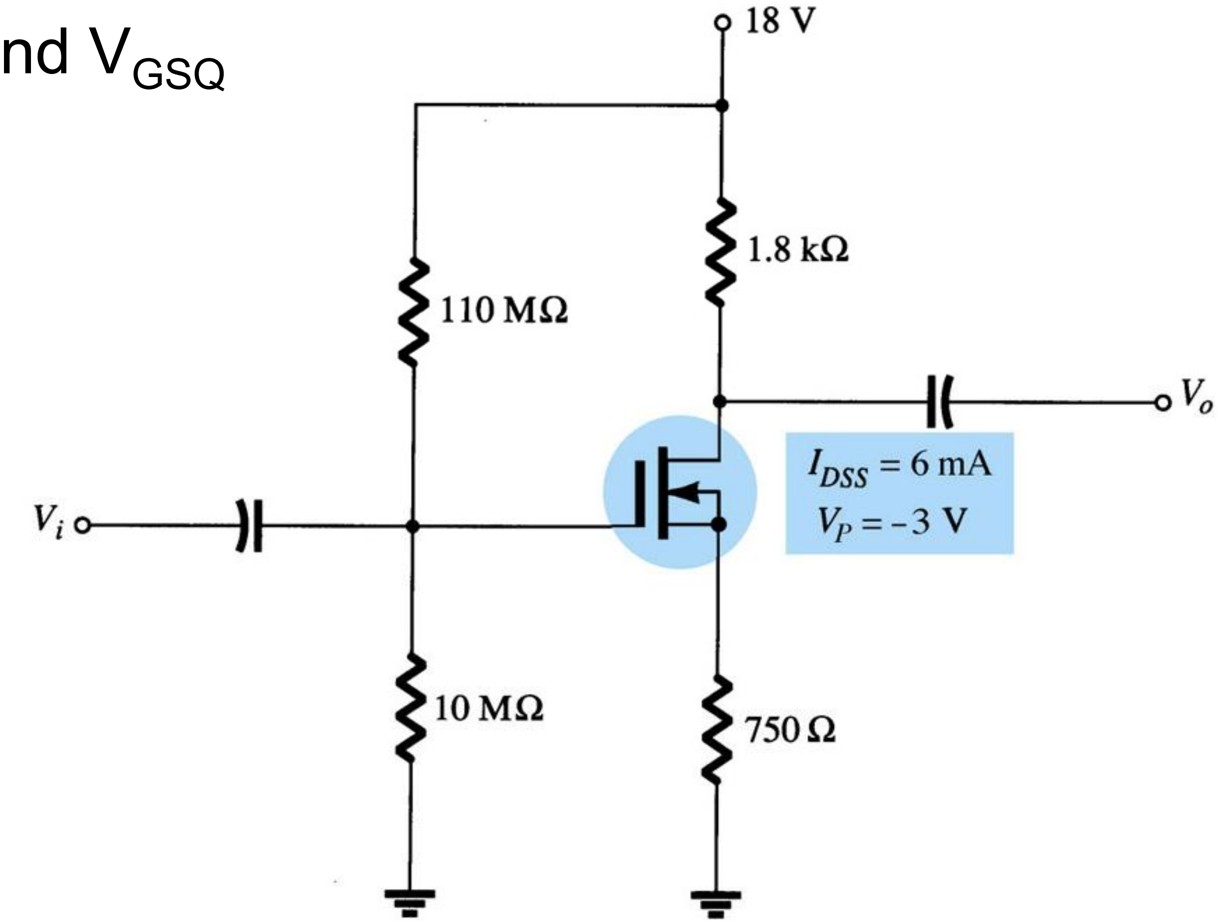


Biasing Circuits

- Same with JFET's fixed-bias configuration except for the device is change to depletion-type MOSFET device
- All the calculation are the same as in JFET, but an extra point when plotting for the transfer curve for positive value of V_{GS}

Example 7.7

- Determine I_{DQ} and V_{GSQ}
- Determine V_{DS}



Example 7.7

- All the calculation for voltage-divider bias configuration are all the same as in JFET's voltage-divider bias configuration
- First, calculate V_G:

$$\therefore V_G = 18 * \frac{10M}{10M + 110M} = 1.5\ V$$

- For V_S:

$$I_S = I_D$$
$$\therefore V_S = 750 I_D$$

- So, for V_{GS}: $V_{GS} = V_G - V_S = 1.5 - 750 I_D$

Example 7.7

- Calculating I_D using Shockley's equation:

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 6m\left(1-\frac{1.5-750I_D}{-3}\right)^2$$

$$\therefore 375{I_D}^2 - 5.5I_D + 13.5m = 0$$

- Solving the equation, we get:

$$I_D = \frac{-b\pm\sqrt{b^2-4ac}}{2a} = \frac{5.5\pm\sqrt{(-5.5)^2-4(375)(13.5m)}}{2(375)}$$

$$= 11.55\text{ mA and } 3.12\text{ mA}$$

Example 7.7

- Even though it seems that the value I_D = 3.12mA is acceptable due to the value I_D = 11.55mA has exceed the limit of I_{DSS}, but remember that I_D can exceed I_{DSS} for depletion-type MOSFET
- To make sure which value is acceptable, check the value by inserting into the V_{GS} equation:

$$V_{GS} = 1.5 - 750 I_D$$

$$\text{For } I_D = 11.55\text{ mA}, V_{GS} = 1.5 - 750(11.55m) = -7.16\text{ V}$$

$$\text{For } I_D = 3.12\text{ mA}, V_{GS} = 1.5 - 750(3.12m) = -0.84\text{ V}$$

- From the result above, for I_D = 11.55 mA, the V_{GS} obtained has exceed the limit of V_P = - 3 V. Thus, the value for I_D = 3.12 mA is taken

Example 7.7

- Using the graphical approach to get the Shockley's curve:

V_{GS}	I_{DD}
0 V	I_{DSS} = 6 mA
$0.3V_P$ = -0.9 V	$I_{DSS}/2$ = 3 mA
$0.5V_P$ = -1.5 V	$I_{DSS}/4$ = 1.5 mA
V_P = -3 V	0 mA

- For the extra plot point when V_{GS} is a positive value, take V_{GS} = +1V due to V_P = -3V and when V_{GS} is positive it rise more rapidly
- Using Shockley's equation, for V_{GS} = +1V, I_D = 10.67mA

Example 7.7

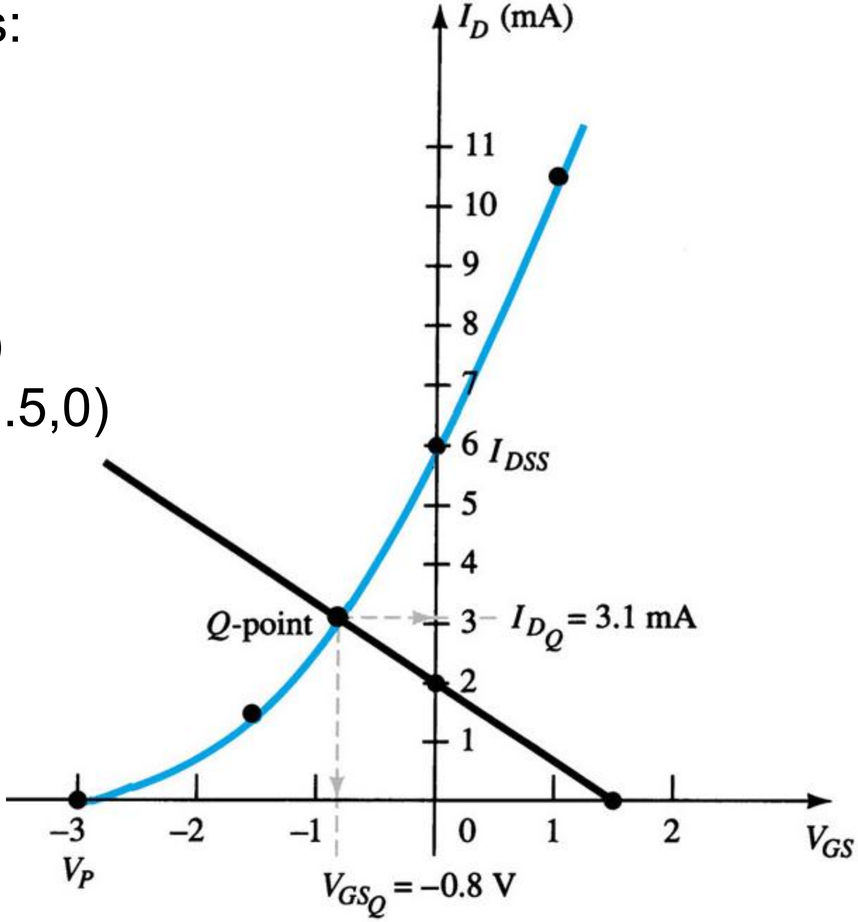
From the circuit, equation of V_{GS} is:

$$V_{GS} = 1.5 - 750I_D$$

Take two points for plotting:

If V_{GS} = 0 V, I_D = 2 mA ➔ (0,2)
If I_D = 0 mA, V_{GS} = 1.5 V, ➔ (1.5,0)

- The Q-point is at $I_D \approx 3.1$ mA which is very close to the value of I_D obtained by using mathematical approach



Example 7.8

Repeat Example 7.7 with R_S = 150 Ω

- The value of V_G is still the same due to V_{DD}, R_1 and R_2 are still the same. V_G = 1.5 V
- For V_S:

$$I_S = I_D = \frac{V_S}{R_S} = \frac{V_S}{150}$$

$$\therefore V_S = 150 I_D$$

- Calculating I_D using Shockley's equation:

$$V_{GS} = V_G - V_S = 1.5 - 150 I_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 6m\left(1 - \frac{1.5 - 150 I_D}{-3}\right)^2$$

$$\therefore 15 I_D^{\ 2} - 1.9 I_D + 13.5m = 0$$

Example 7.8

- Solving the equation, we get:

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{1.9 \pm \sqrt{(-1.9)^2 - 4(15)(13.5m)}}{2(15)}$$

$$= 119.11\,\text{mA and } 7.56\,\text{mA}$$

- It seems that both the value for I_D have exceed the limit of I_{DSS}. Remember that I_D can exceed I_{DSS} for depletion-type MOSFET. To make sure which one is acceptable, insert both value into the V_{GS} equation:

$$V_{GS} = 1.5 - 150 I_D$$

$$\text{For } I_D = 119.11\,\text{mA}, V_{GS} = 1.5 - 150(119.11m) = -16.37\text{ V}$$

$$\text{For } I_D = 7.56\,\text{mA}, V_{GS} = 1.5 - 150(7.56m) = 0.37\text{ V}$$

Example 7.8

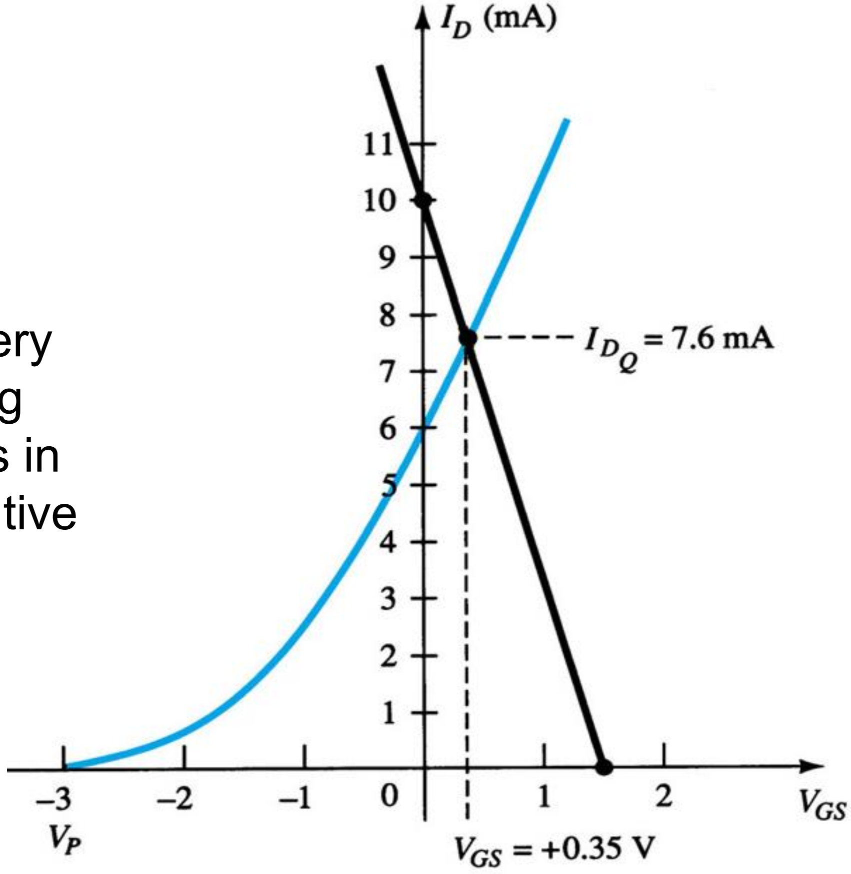
- From the result above, for I_D = 119.11 mA, the V_{GS} obtained has exceed the limit of V_P = - 3 V. Thus, the value for I_D = 7.56 mA is taken
- Notice that when I_D = 7.56 mA, the value of V_{GS} = 0.37 V. If the value of V_{GS} is positive, it means that I_D is in the enhancement region
- This will be confirmed when obtaining the values with graphical approach

Example 7.8

- From the circuit, equation of V_{GS} is: $V_{GS} = 1.5 - 150 I_D$
- Take two points for plotting:

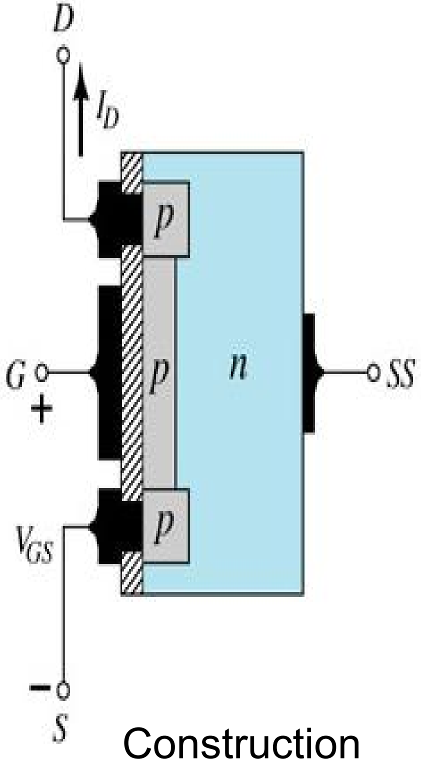
  -If V_{GS} = 0 V, I_D = 10 mA ➔ (0,10)

  -If I_D = 0 mA, V_{GS} = 1.5 V, ➔ (1.5,0)

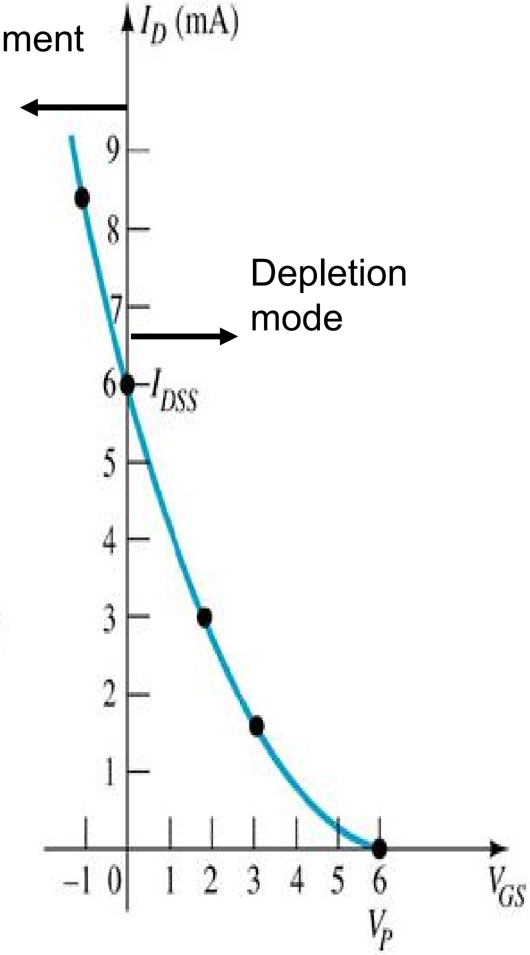


The Q-point is at $I_D \approx 7.6$ mA which is very close to the value of I_D obtained by using mathematical approach. Notice that I_D is in the enhancement region due to the positive value of V_{GS}

p-Channel Depletion-Type MOSFET



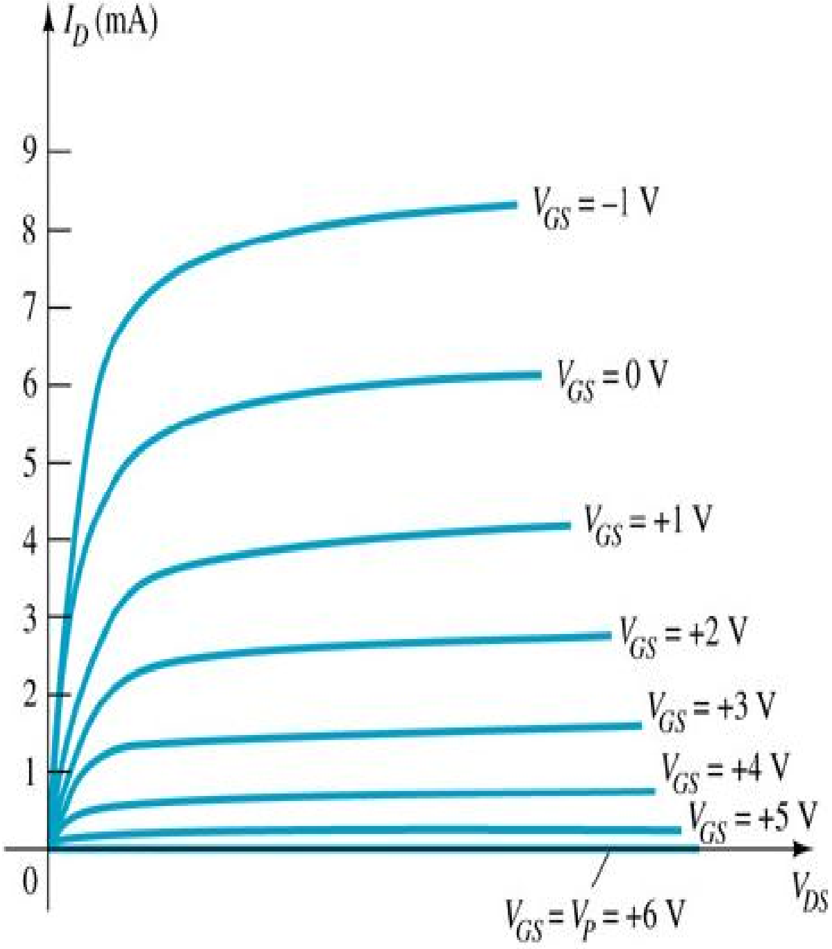
Construction



Enhancement mode

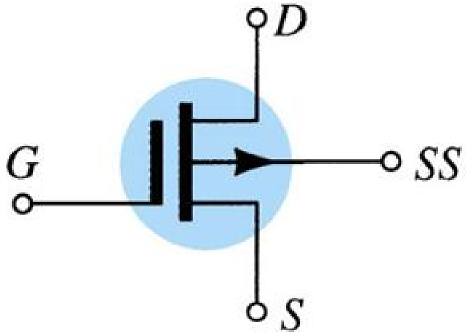
Depletion mode

Transfer Curve

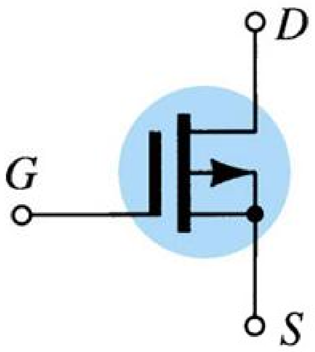


Characteristics

p-Channel Depletion-Type MOSFET Symbol

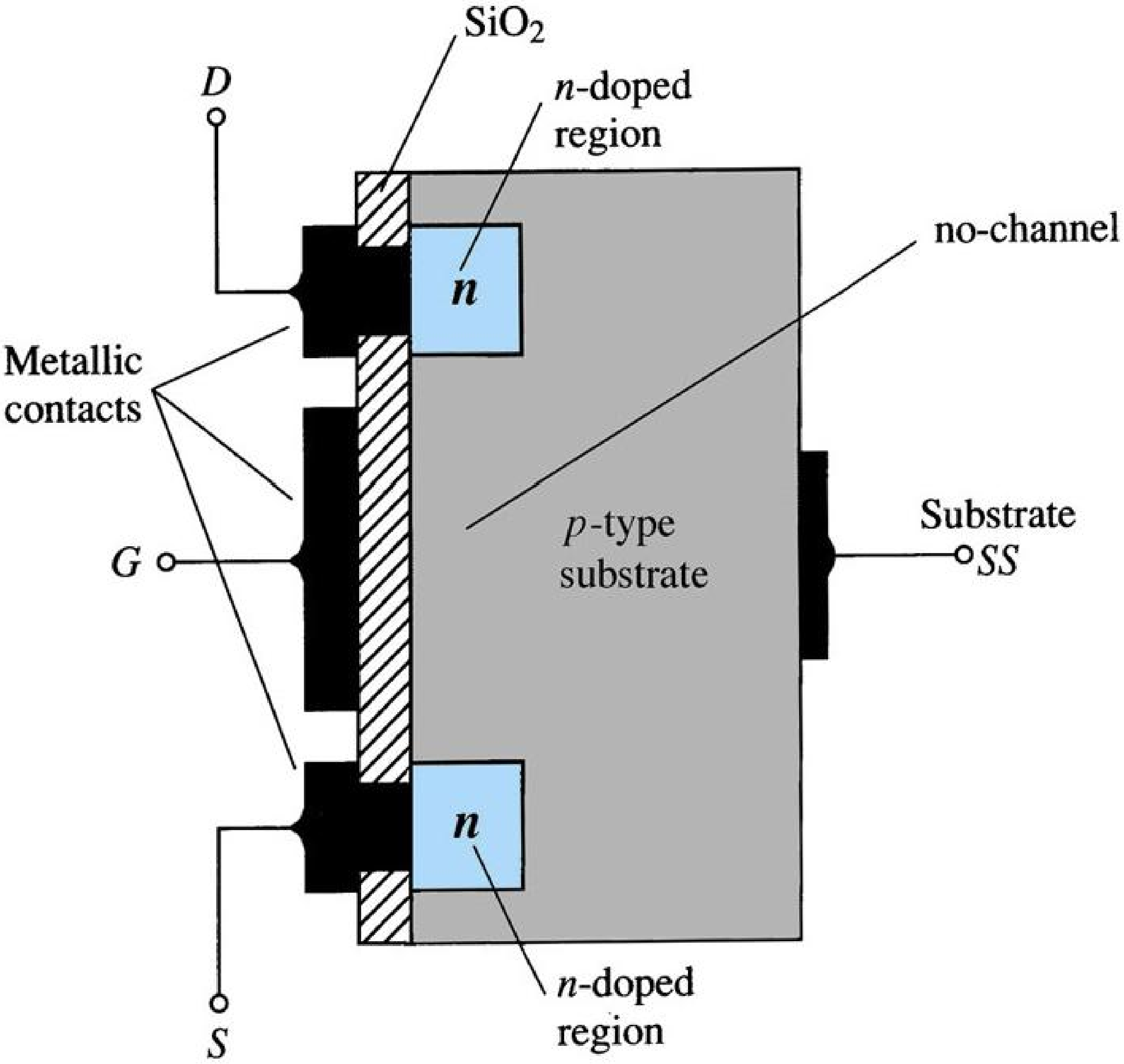


or



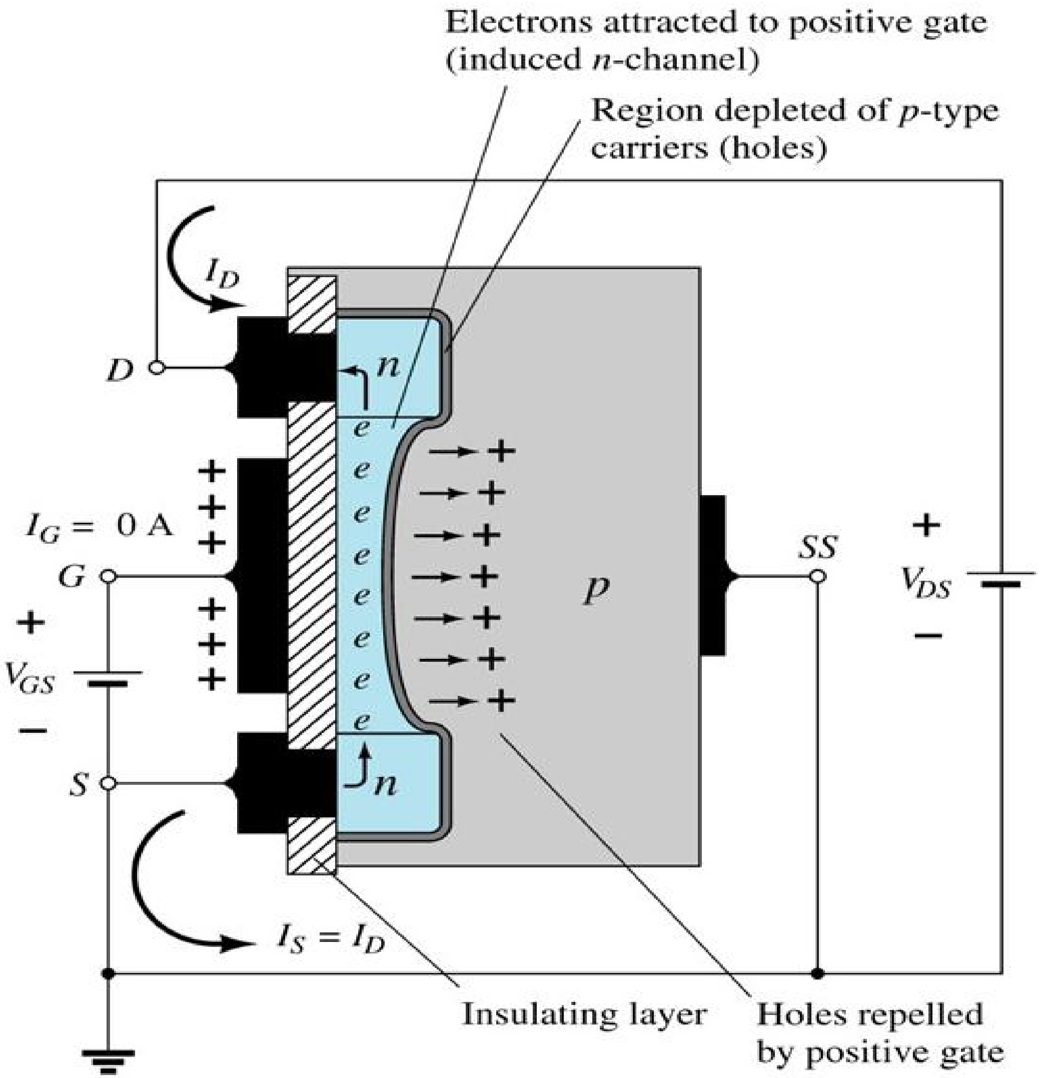
Enhancement-Type MOSFET Construction

- As usual, n-channel enhancement-type MOSFET will be discussed first
- The device is the same as depletion-type MOSFET, but notice that there is no channel between the drain and source terminal



Enhancement-Type MOSFET Operation

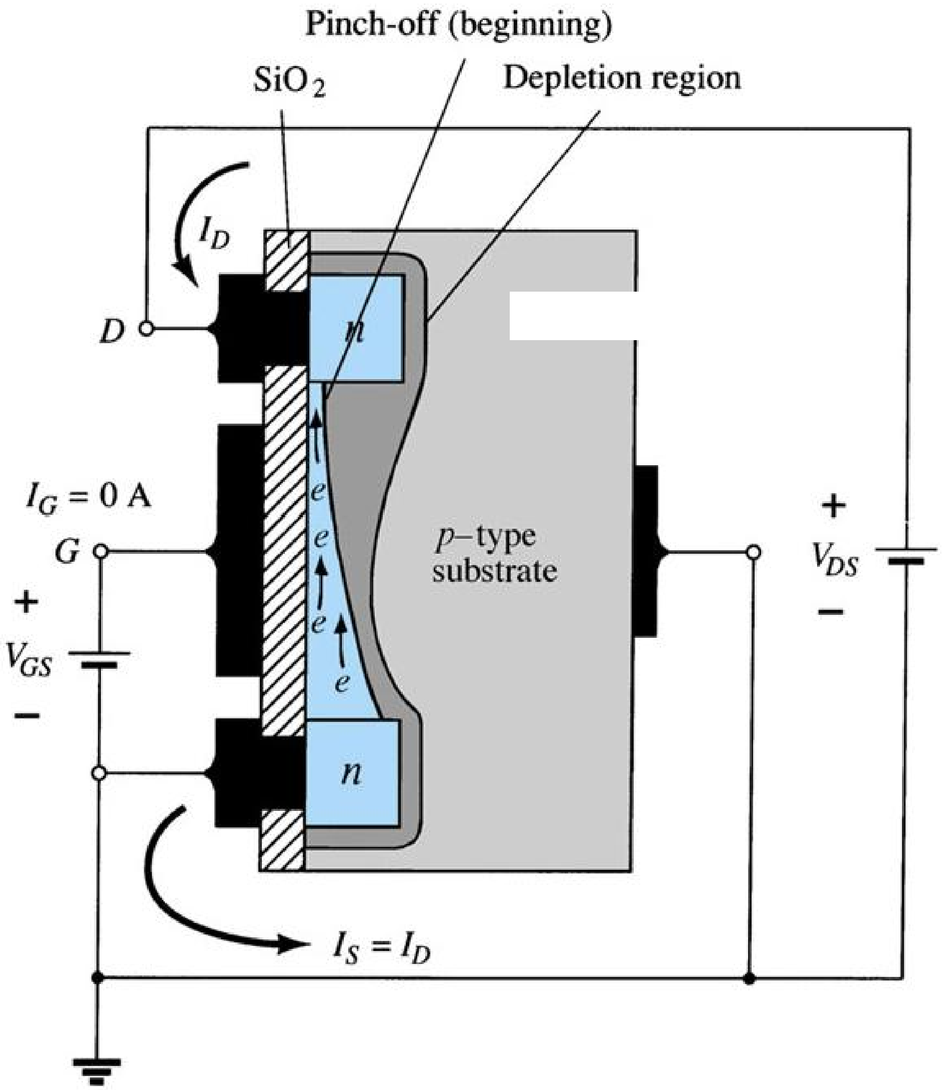
- Because there is no channel, so no current will flow no matter what voltage applied (V_{DD}) to the drain and source terminal ($I_D = 0$ for $V_{GS} < V_T$)
- So, a certain voltage (threshold voltage, V_T) must be applied to the gate terminal so that a channel will develop and the current will flow between drain and source terminal



Enhancement-Type MOSFET Operation

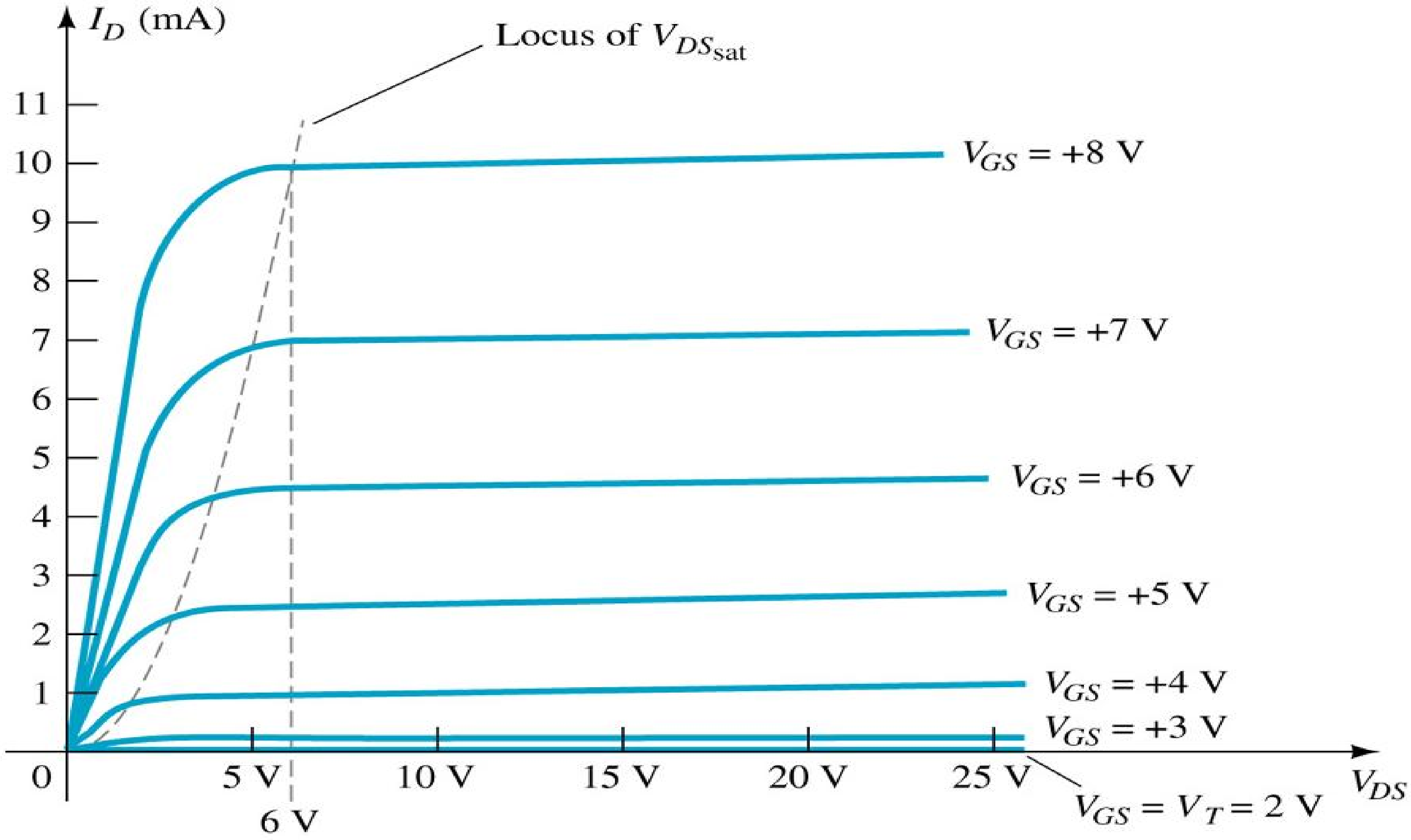
- By setting V_G higher than V_T, a channel will develop
- As for that, when V_{DS} (formerly known as V_{DD}) is increased, the pinch-off situation will happen and a saturation current I_{DSS} will be obtained (same as in JFET and depletion-type MOSFET)
- Pinch-off voltage $V_{DS(sat)}$ (formerly known as V_P) will became higher when V_G is increase due to the widening of the channel developed
- The pinch-off or saturation voltage obtain is defined by the equation:

$$V_{DS(sat)} = V_{GS} - V_T$$



Enhancement-Type MOSFET Characteristic

- The characteristic of the enhancement-type MOSFET would be:



Enhancement-Type MOSFET Characteristic

- The transfer curve is not define by Shockley's equation anymore. It is defined by the equation:

$$I_D = k(V_{GS} - V_T)^2 \text{ for } V_{GS} \geq V_T$$

- Where k is defined by:

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

- The term (on) means that the values where the device has reached its saturation level
- As for the example of the characteristic curve given, the (on) values are $V_{GS(on)}$=+8V where $I_{D(on)}$=10mA or $V_{GS(on)}$=+7V where $I_{D(on)}$=7mA or $V_{GS(on)}$=+6V where $I_{D(on)}$≈4.5mA or any other values that have reached saturation level

Enhancement-Type MOSFET Characteristic

- Usually, we take the highest saturation level shown in the graph
- So, the value of k for the characteristic example given above is:

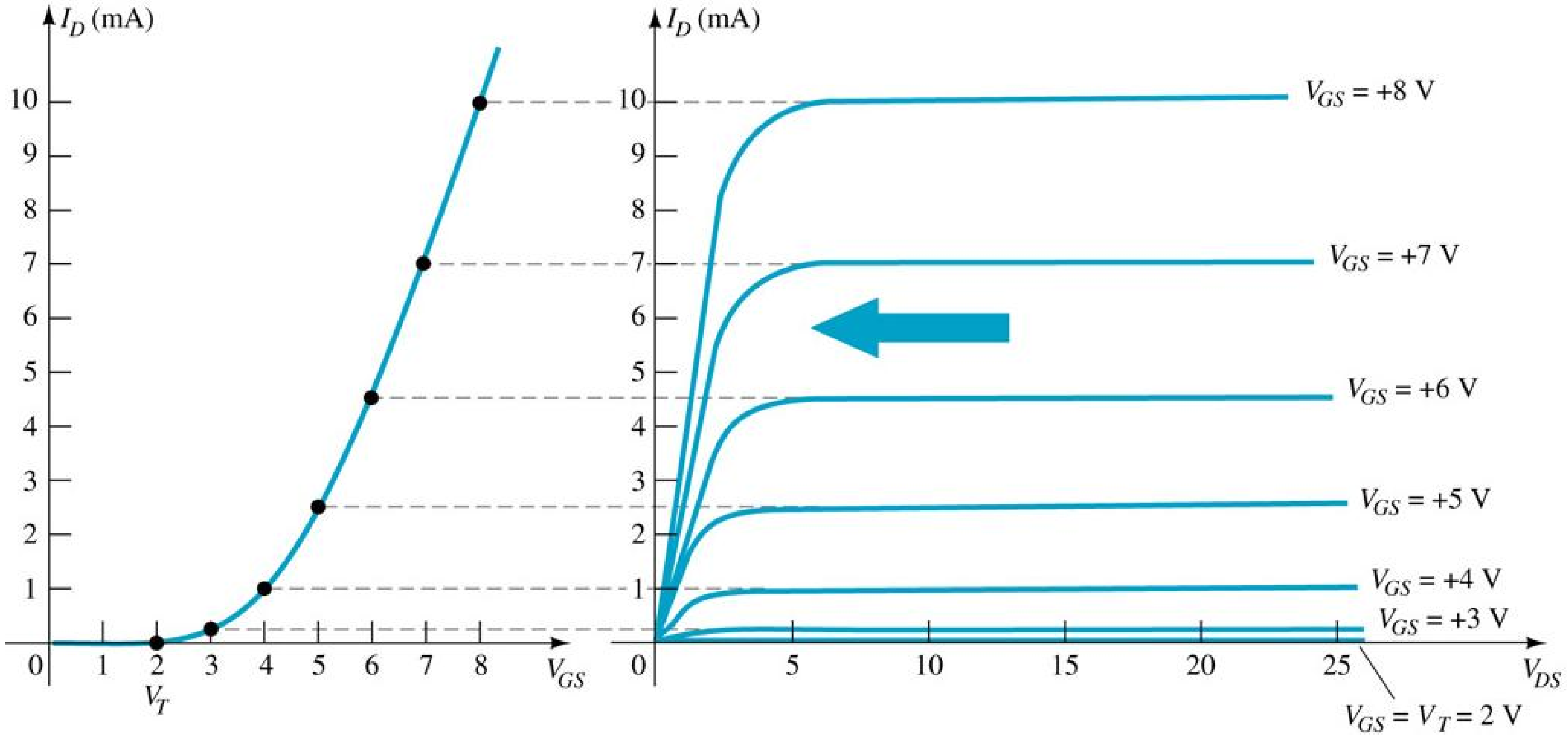
$$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_T\right)^2} = \frac{10m}{(8-2)^2} = 0.278\,\mathrm{mA/V}^2$$

- Notice the unit of k is in $\mathrm{mA/V}^2$ because the numerator is current and the denumerator is voltage^2
- So, the I_D equation for this example will become:

$$I_D = 0.278m\left(V_{GS} - 2\right)^2$$

Enhancement-Type MOSFET Transfer Curve

- Plotting all the $V_{DS(sat)}$ from the characteristic curve, the transfer curve can be obtained:



Example for Plotting the Transfer Curve

- Plot the transfer curve for the device that have the characteristic of:

- Firstly, for $V_{GS} \leq 4$, all I_D will be 0 A

$$I_D = 0.5m\left(V_{GS} - 4\right)^2$$

- Taking one step after the point of V_T, $V_{GS} = 5$ V resulting in
- :

$$I_D = 0.5m\left(V_{GS} - 4\right)^2 = 0.5m\left(5 - 4\right)^2 = 0.5\ \mathrm{mA}$$

- Next, one step after that, $V_{GS} = 6$ V, resulting in:

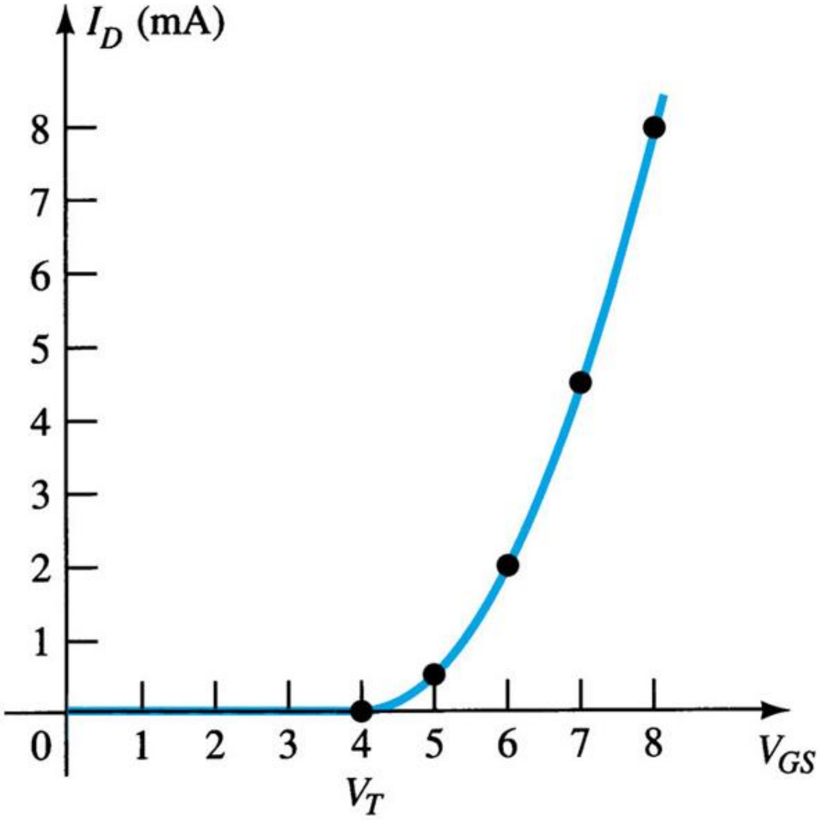
$$I_D = 0.5m\left(V_{GS} - 4\right)^2 = 0.5m\left(6 - 4\right)^2 = 2\ \mathrm{mA}$$

- Continue the steps until to an appropriate value

Example for Plotting the Transfer Curve

- Plots the transfer curve:

V_{GS}	I_D
5 V	0.5 mA
6 V	2 mA
7 V	4.5 mA
8 V	8 mA



Important Relationships

$$I_G = 0$$

$$I_D = I_S$$

$$I_D = k\left(V_{GS} - V_T\right)^2 \text{ for } V_{GS} \geq V_T$$

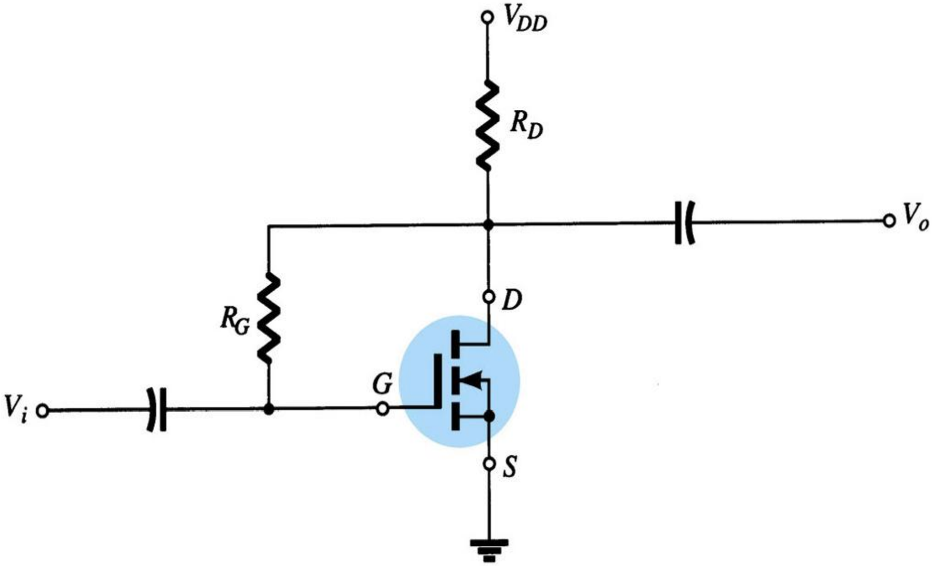
$$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_T\right)^2}$$

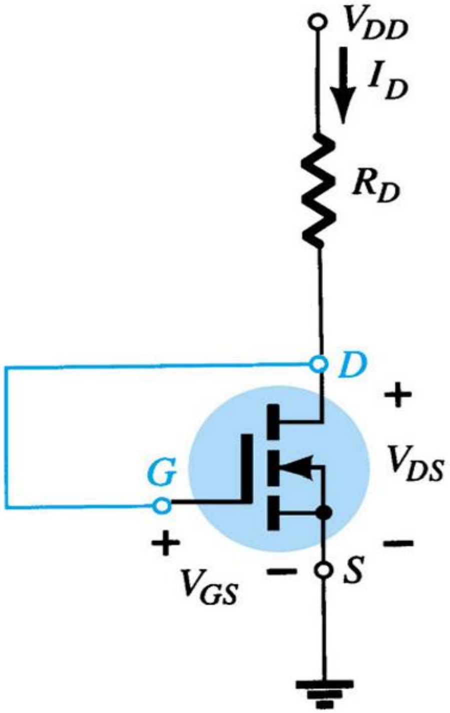
Enhancement-Type MOSFET DC Biasing

- Although the fixed-bias, self-bias and many more bias configuration can be applied to enhancement-type MOSFET, but there only two biasing that is very popular for this kind of MOSFET
- Those 2 most popular bias configuration are:

1. Feedback-bias configuration
2. Voltage-divider bias configuration

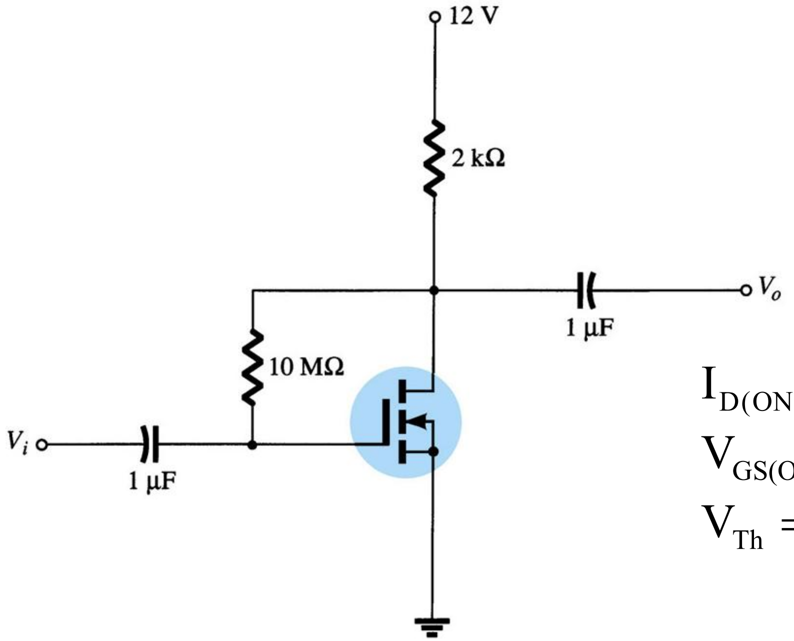
Feedback-Bias Configuration





As the situation $I_G = 0$ still applied, the resistor R_G will be ignored resulting in the drain and gate terminal to have the same voltage ($V_G = V_D$)

Example 7.11



$$I_{D(ON)} = 6\,\text{mA}$$
$$V_{GS(ON)} = 8\,\text{V}$$
$$V_{Th} = 3\,\text{V}$$

For the enhancement-type MOSFET's equation, the value of k have to be obtained first:

$$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_T\right)^2} = \frac{6m}{(8-3)^2} = 0.24\,\text{mA/V}^2$$

the I_D equation for the device: $I_D = 0.24m\left(V_{GS} - 3\right)^2 \text{ for } V_{GS} \geq 3$

Example 7.11

$$\mathrm{V_G = V_D = 12 - 2kI_D}$$

- Inserting the V_{GS} equation into the device equation:

$$V_{GS} = V_G - V_S = 12 - 2kI_D - 0 = 12 - 2kI_D$$

$$I_D = 0.24m(V_{GS} - 3)^2 = 0.24m(12 - 2kI_D - 3)^2 = 0.24m(9 - 2kI_D)^2$$
$$= 0.24m\left(81 - 36kI_D + 4MI_D{}^2\right) = 19.44m - 8.64I_D + 960I_D{}^2$$
$$\therefore 960I_D{}^2 - 9.64I_D + 19.44m = 0$$

Example 7.11

- Solving the equation, we get:

$$I_D = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} = \frac{9.64 \pm \sqrt{(-9.64)^2 - 4(960)(19.44m)}}{2(960)}$$

$$= 7.25\,\mathrm{mA}\ \text{and}\ 2.79\,\mathrm{mA}$$

- Due to enhancement-type MOSFET doesn't have limitation for saturation current (I_{DSS}), the true value of I_D is the smaller one

$$\mathrm{I}_{\mathrm{D_Q}} = 2.79\,\mathrm{mA}$$

$$\text{and}\quad \mathrm{V_{GS}} = 12 - 2\mathrm{kI_D} = 6.42\,\mathrm{V}$$

Example 7.11

- For graphical approach, several plot points have to be obtained first:

$$I_D = 0.24m(V_{GS} - 3)^2 \text{ for } V_{GS} \geq 3$$

V_{GS}	I_D
3 V	0 mA
4 V	0.24 mA
5 V	0.96 mA
6 V	2.16 mA
7 V	3.84 mA
8 V	6 mA

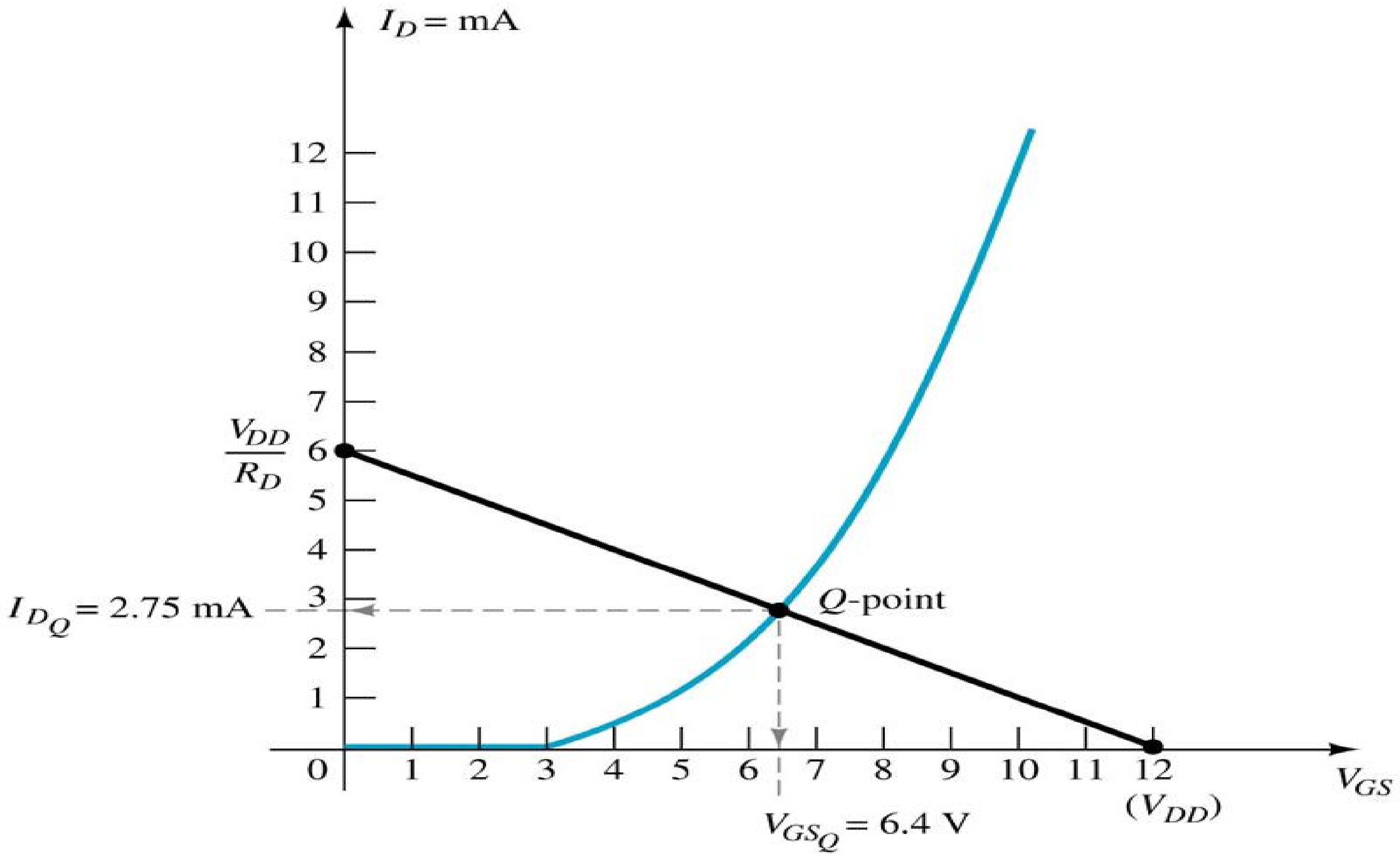
- For the bias line, only two plot points are required:

$$V_{GS} = 12 - 2kI_D$$

V_{GS}	I_D
12 V	0 mA
0 V	6 mA

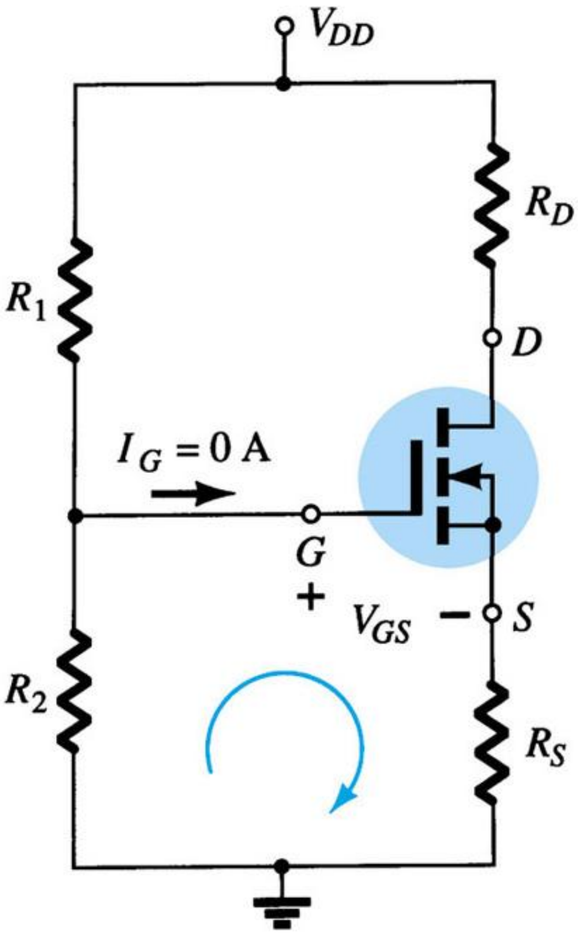
Example 7.11

- Plots all the device transfer curve and device representation points:



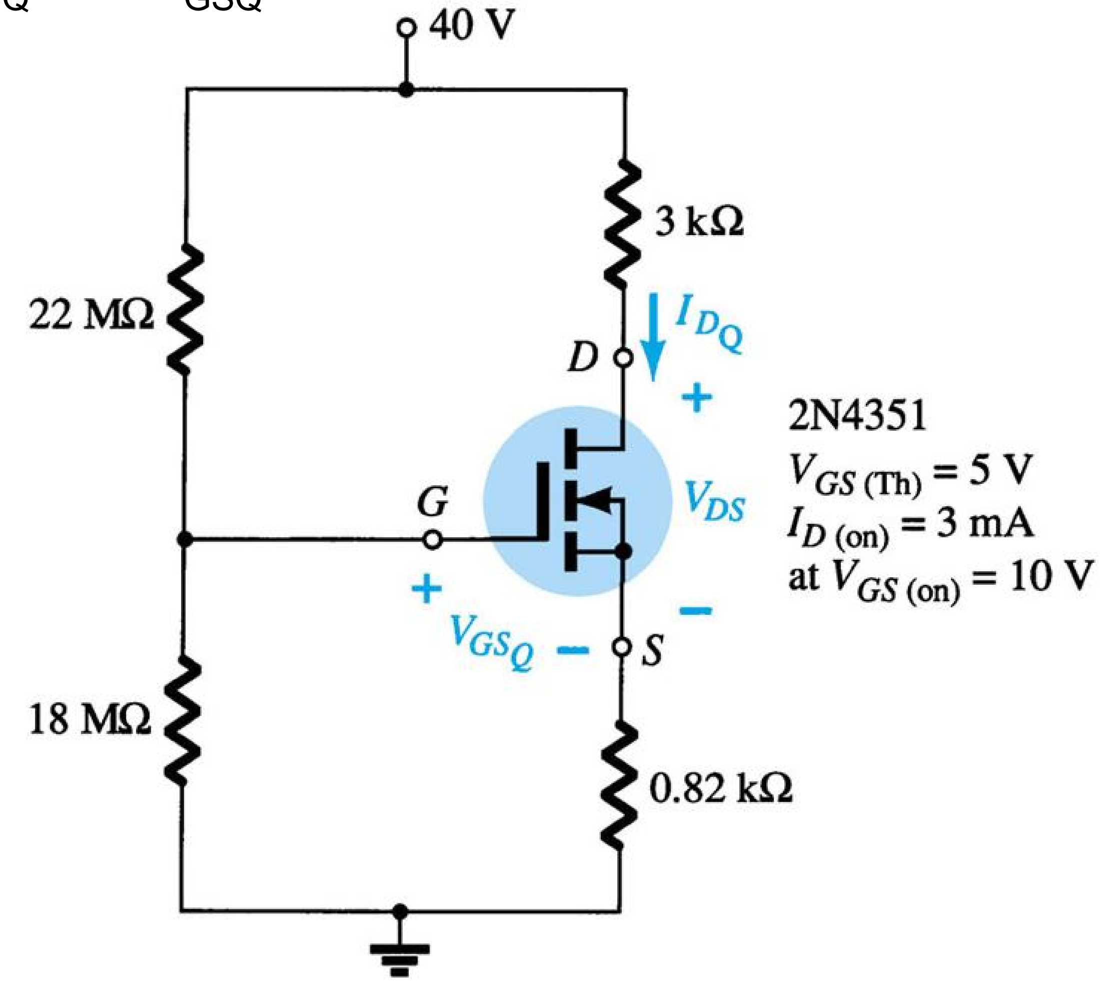
Voltage-Divider Bias Configuration

- Basically, the configuration is the same as in depletion-type MOSFET, JFET or BJT except the change of device to the enhancement-type MOSFET
- All the calculation would be the same except for the transfer curve of enhancement-type MOSFET is different from those depletion-type MOSFET and JFET



Example 7.12

- Determine I_{DQ} and V_{GSQ}



Example 7.12

- Determining V_G: $$V_G = 40 * \frac{18\text{M}}{18\text{M} + 22\text{M}} = 18\text{ V}$$
- For V_S: $V_S = 0.82\text{kI}_D$
- So, for V_{GS}: $V_{GS} = V_G - V_S = 18 - 0.82kI_D$

Determining k: $$k = \frac{I_{D(on)}}{\left(V_{GS(on)} - V_T\right)^2} = \frac{3m}{(10-5)^2} = 0.12\text{ mA/V}^2$$

Inserting the circuit representation equation into the device equation:

$$I_D = 0.12m\left(V_{GS} - 5\right)^2 \text{ for } V_{GS} \geq 5$$

$$I_D = 0.12m\left(V_{GS} - 5\right)^2 = 0.12m\left(18 - 0.82kI_D - 5\right)^2$$

$$\therefore 80.69{I_D}^2 - 3.56I_D + 20.28m = 0$$

Example 7.12

- Solving the equation, we get:

$$\mathrm{I_D} = \frac{-\mathrm{b} \pm \sqrt{\mathrm{b}^2 - 4\mathrm{ac}}}{2\mathrm{a}} = \frac{3.56 \pm \sqrt{(-3.56)^2 - 4(80.69)(20.28\mathrm{m})}}{2(80.69)}$$

$$= 37.4\ \mathrm{mA\ and}\ 6.72\ \mathrm{mA}$$

We take the smaller value: $\mathrm{I_D} = 6.72\ \mathrm{mA}$

$$\mathrm{V_{GS}} = 18 - 0.82\mathrm{kI_D}$$

$$\mathrm{For\ I_D} = 6.72\ \mathrm{mA},\ \mathrm{V_{GS}} = 18 - 0.82\mathrm{k}(6.72\mathrm{m}) = 12.49\ \mathrm{V}$$

$$I_{D_Q} = 6.72\ \mathrm{mA}$$

$$V_{GS_Q} = 12.49\ \mathrm{V}$$

Example 7.12

- For graphical approach, several plot points have to be obtained first:

$$I_D = 0.12m\left(V_{GS} - 5\right)^2 \text{ for } V_{GS} \geq 5$$

V_{GS}	I_D
5 V	0 mA
10 V	3 mA
15 V	12 mA
20 V	27 mA
25 V	48 mA
30 V	75 mA

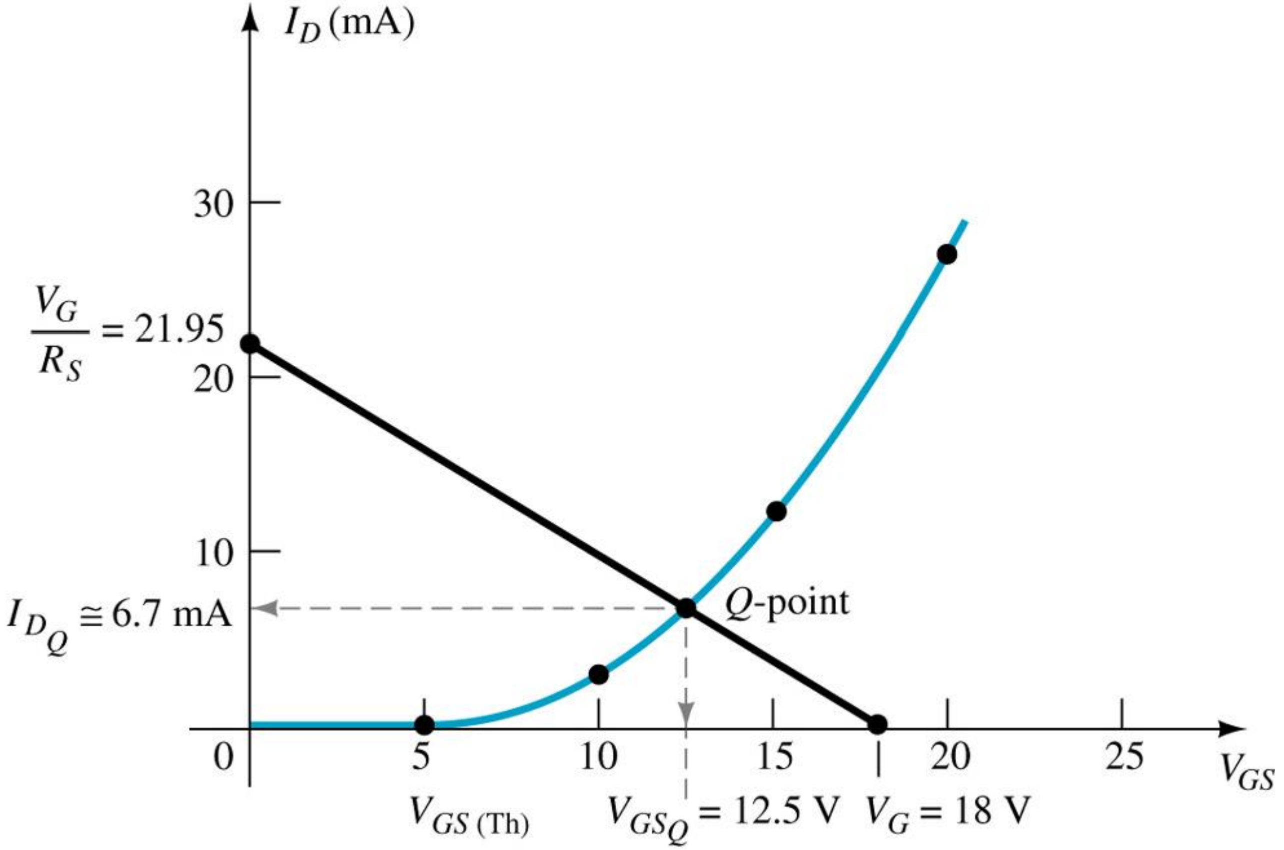
- For the bias line, only two plot points are required:

$$V_{GS} = 18 - 0.82kI_D$$

V_{GS}	I_D
18 V	0 mA
0 V	21.95 mA

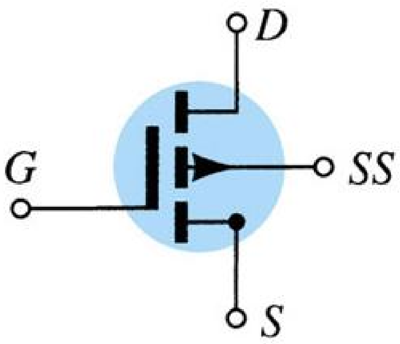
Example 7.12

- Plots all the device transfer curve and device representation points:

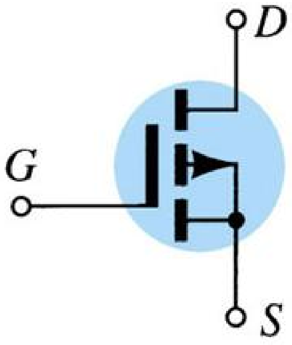


p-Channel Enhancement-Type MOSFET

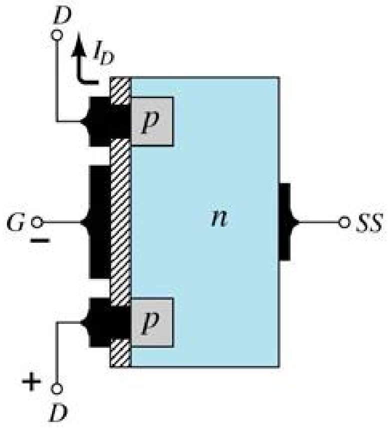
- It is the complement to *n*-channel enhancement-type MOSFET
- All the current flow will be in the opposite direction
- Although the current direction is reverse, however the current equation are still the same (just like in JFET and depletion-type MOSFET)
- *p*-channel enhancement-type symbol:



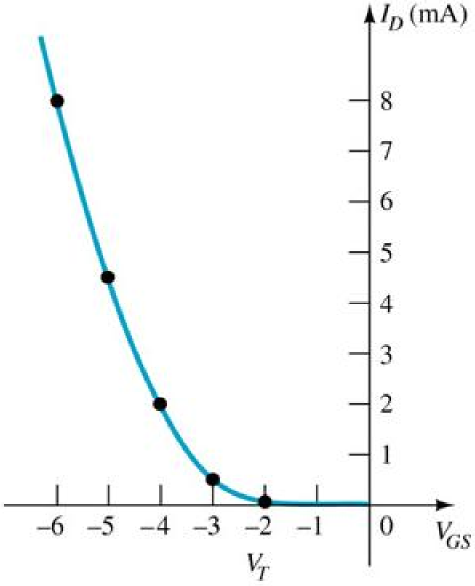
or



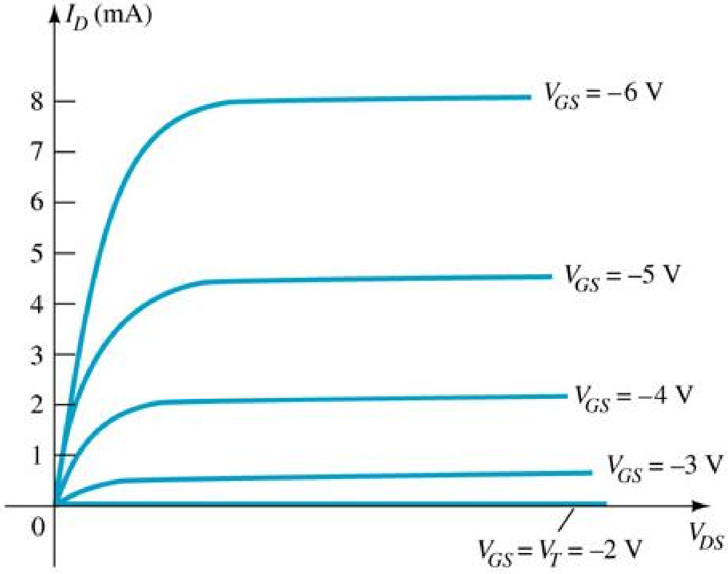
p-Channel Enhancement-Type MOSFET



Construction



Transfer Curve



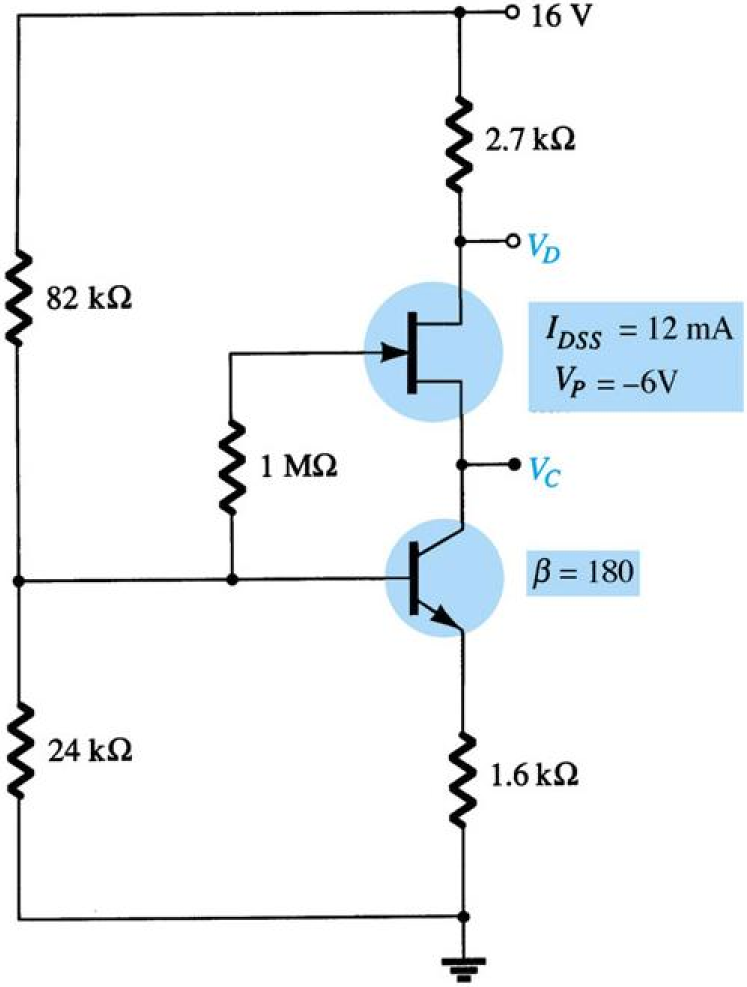
Characteristics

Combination Networks

- Combination of BJT and FET device in a circuit
- Firstly, recognize both of the devices and their current flows
- To make the calculation simple and easier to view, transform the circuit into the equivalent form to avoid complexity
- List down all the important relationships that involve for both of the devices
- Start with approaching the device that is closer to the ground (bottom device)

Example 7.13

- Determine V_D and V_C



Example 7.13

- We know that for the JFET device, $I_G = 0$ making the resistor $R_G = 1\ \text{M}\Omega$ useless and can be remove from the circuit

- By analyzing the circuit, we notice that the configuration is a voltage-divider bias for both the JFET and BJT device

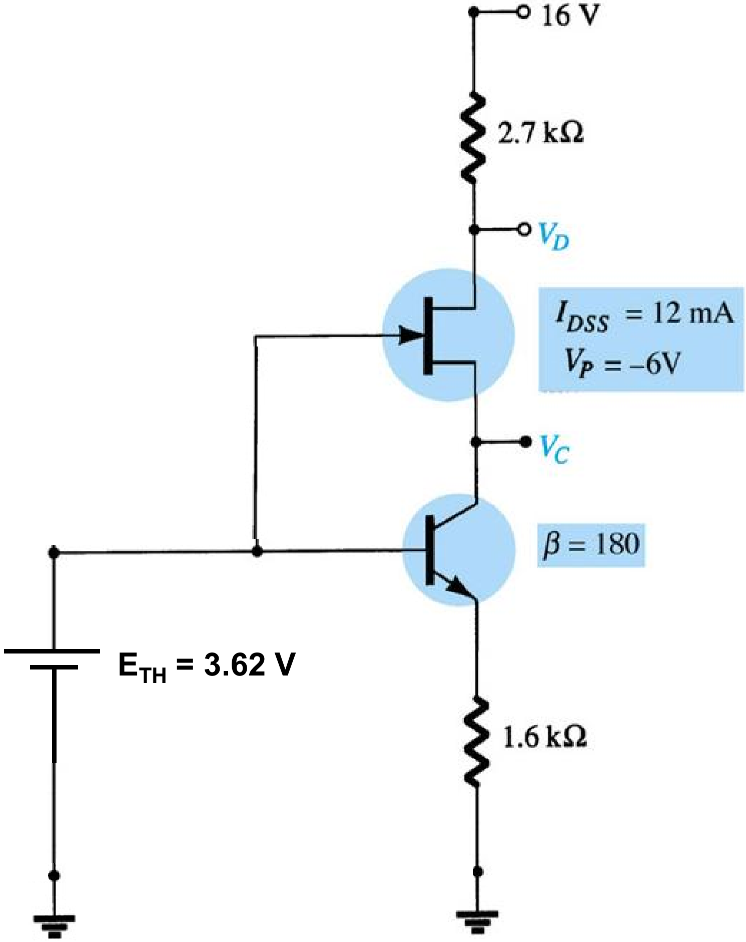
- Due to involvement of BJT, we have to check $\beta R_E \geq 10R_2$ to use the approximate analysis

- As for $\beta R_E = (180)(1.6k) = 288k$ and $10R_2 = 10(24k) = 240k$, situation $\beta R_E \geq 10R_2$ is satisfied and we can use approximate analysis for this configuration
- Obtaining the E_{TH}:

$$\therefore E_{TH} = 16 * \frac{24}{24 + 82} = 3.62\ \text{V}$$

Example 7.13

- Transforming the circuit into its equivalent form:



Example 7.13

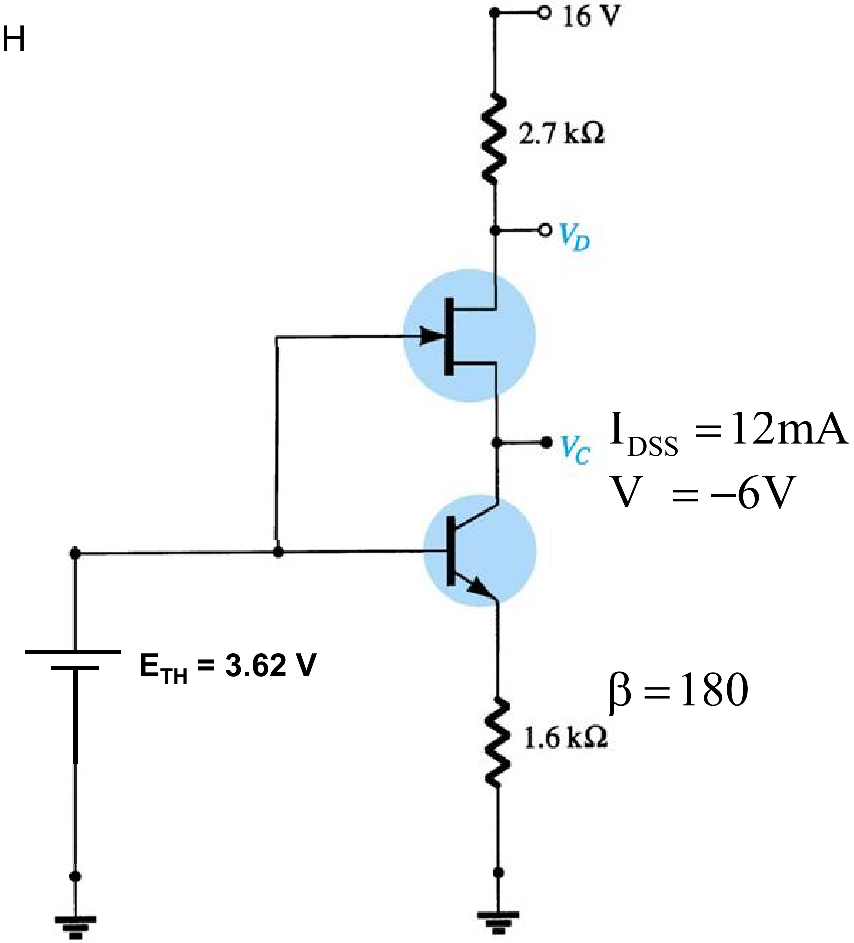
- By approaching BJT (bottom device) first, we know V_{BE} = 0.7
- From earlier calculation, we got E_{TH}
- Obtaining V_E:

$$\therefore V_E = I_E * R_E = (\beta + 1) I_B * R_E =$$

$$181 I_B * 1.6k = 289.6k I_B$$

- Obtaining I_B from V_{BE} = 0.7:

$$V_{BE} = V_B - V_E = 0.7$$
$$0.7 = 3.62 - 289.6k I_B$$
$$\therefore I_B = 10.08\,\mu A$$



Example 7.13

- From the circuit, I_B is not really important but I_C is very important because
- $I_C = I_S = I_D$
- As for that, obtain I_C:

$$I_C = \beta I_B = (180)(10.08\mu) = 1.81\,\mathrm{mA}$$

- Knowing the value of I_D, V_D can be obtained:

$$\therefore \mathrm{V_D} = 16 - \mathrm{I_D} * 2.7\mathrm{k} = 11.11\,\mathrm{V}$$

Example 7.13

- From the configuration, we notice that $V_S = V_C$
- By obtaining V_{GS} for the JFET, the value of V_S can be achieved:

$$V_{GS} = V_G - V_S = 3.62 - V_S = 3.62 - V_C$$

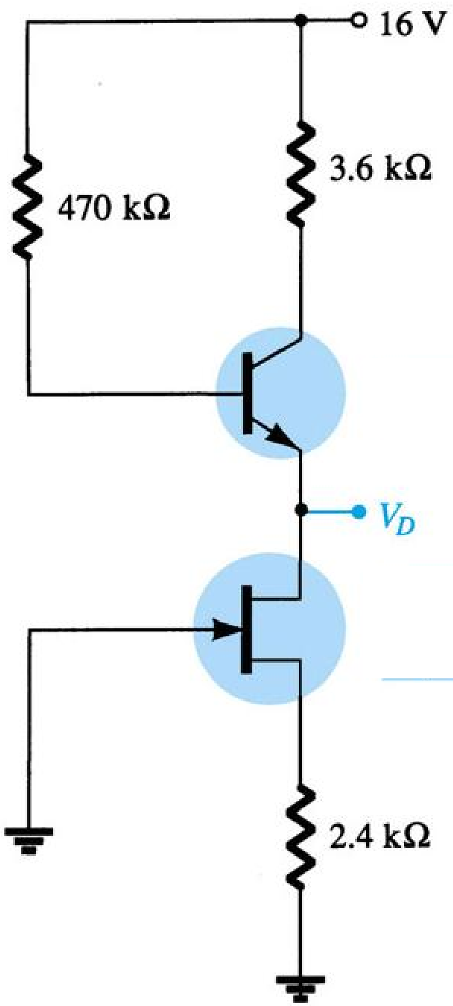
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$1.81m = 12m\left(1 - \frac{3.62 - V_C}{-6}\right)^2$$

$$\therefore V_C = 7.29 \text{ V}$$

Example 7.14

- Determine V_D:



$\beta = 80$

$I_{DSS} = 8mA$
$V_p = -6V$

Example 7.14

- Approaching the JFET (bottom device) first, obtain V_{GS} to be used with Shockley's equation:

$$V_G = 0$$

$$I_D = I_S = \frac{V_S}{2.4k}$$

$$\therefore V_S = 2.4kI_D$$

$$\therefore V_{GS} = V_G - V_S = 0 - 2.4kI_D = -2.4kI_D$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8m\left(1 - \frac{-2.4kI_D}{-4}\right)^2$$

$$\therefore I_D = 1.06\,\text{mA and } V_{GS} = -2.54\ \text{V}$$

Example 7.14

- From the configuration, we notice that

$$I_D = I_E$$

- Thus, I_B can be obtained:

$$I_D = I_E = (\beta+1)I_B$$

$$1.06m = 81 I_B$$

$$\therefore I_B = 13.09\ \mu\text{A}$$

- The base voltage is equal to::

$$\therefore \mathrm{V_B} = 16 - \mathrm{I_B} * 470\mathrm{k} = 9.85\ \mathrm{V}$$

As for $V_D = V_E$, the value can be obtained from $V_{BE} = 0.7$

$$V_{BE} = V_B - V_E = V_B - V_D = 9.85 - V_D = 0.7$$

$$\therefore V_D = 9.15\ \text{V}$$